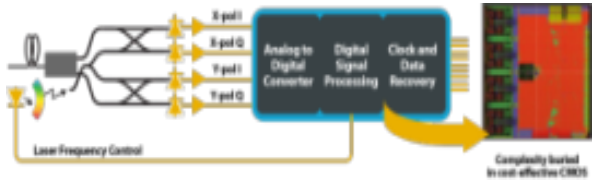
Tektronix

移动产品在数据传输和存储方面的挑战

OCEAN
SENIOR

数字时代趋势和挑战——更高的带宽

高效高速数据和视频网络

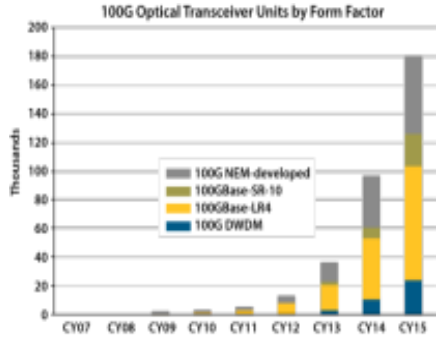


光纤相干位调制

更快、功能更强的消费器件

串行总线标准进化

加快网络服务器接入速度



100Gb/s网络增长

课程安排

- 移动设备的设计挑战
- 热门相关标准
  - 数据存储 - LPDDR
  - 数据传输 - USB（Type C, USB3.1/3.0)
  - 数据传输 - MIPI（M-PHY, D-PHY, C-PHY)
- 总结

移动设备的设计挑战

MIPI D-PHY

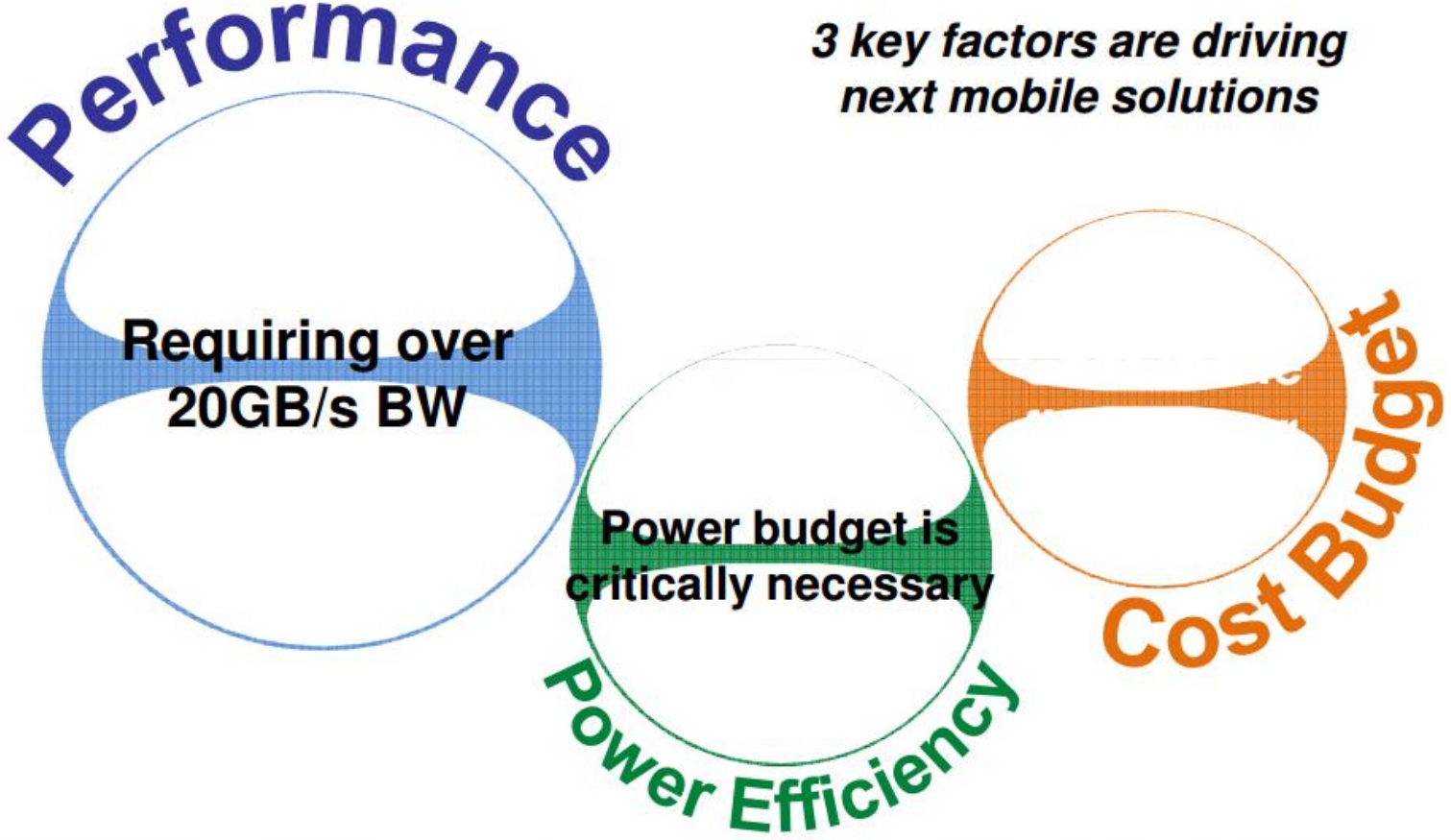
LPDDR

MIPI M-PHY

USB

数据存储 – LPDDR，LPDDR4

Key Factors Driving LPDDR



LPDDR4 Overview

	LPDDR3	LPDDR4	Notes
Channels	1 or 2	2	2 channels per die; LP4 channel = x16 Each LP4 channel has its own CA and Clock CA/Clock/DQ co-located on die
Clock Speed	400MHz to 1066MHz	800MHz to 2133MHz	Doubling the clock rate in LP4
Data Rate	800MT/s to 2133MT/s	1600MT/s to 4267MT/s	Doubling the data rate in LP4
Burst Length	8	16/32	Doubling Pre-fetch, core frequency is same
DQ ODT	No Termination, or 240/120 to VDDQ	VSSQ Termination	VSSQ = Ground
CA ODT	No Termination	VSSQ Termination	VSSQ = Ground
Vref	External	Internal	Vcent replaces Vref as reference for external measurements
Package	PoP/Discrete	PoP/Discrete	No change
I/O Voltage	1.2	1.1	Reduced Voltage
Preamble Postamble	Fixed	User selectable through MR	Makes it complicated to differentiate Read from Write
Voltage Swing	Close to rail/80%	~ 0.4 V	Reduced Swing
Read/Write Timing	Edge / Center Aligned	Edge/not Aligned	Writes need training for DQS to DQ relationship

CA Bus / DQ Bus Vcent

- LPDDR4 bus does not include (externally accessible) VREF.
- Vcent_CAx / Vcent_DQx is the Voltage at which the cumulative eye of the pin CAx / DQx is widest
- Vcent_CA(pin_mid) / Vcent_DQ(pin_mid) is defined as the middle between the largest and smallest Vcent_CA / Vcent_DQ within the group.
- Vcent_CA(pin_mid) / Vcent_DQ(pin_mid) is the best available estimate for the internal VREF (after training), that is accessible at the pins.

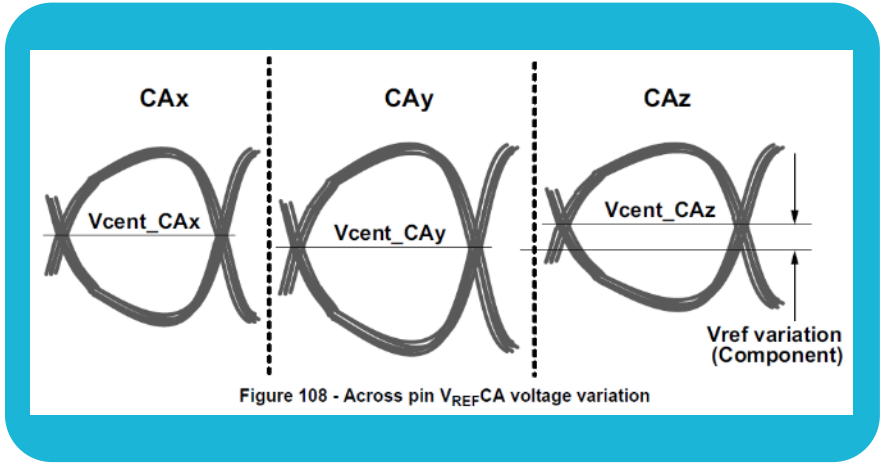


Figure 108 - Across pin $V_{REF}CA$ voltage variation

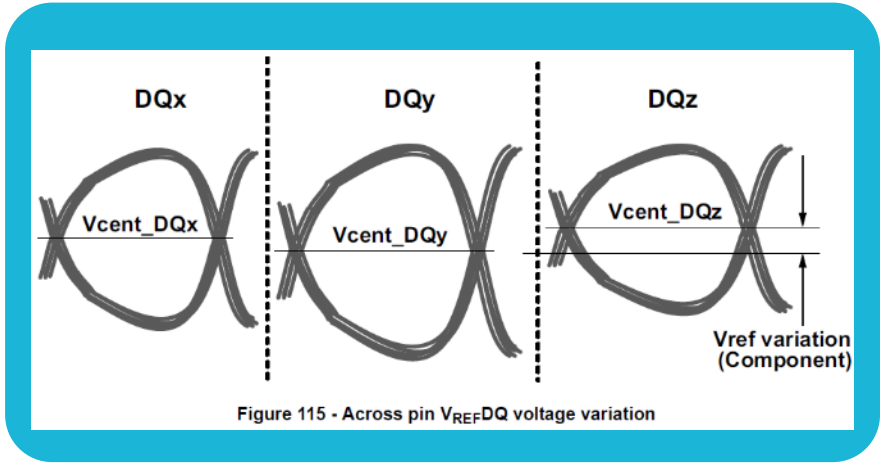


Figure 115 - Across pin $V_{REF}DQ$ voltage variation

CA Bus / DQ Bus Mask-Based Timing and Voltage Definition

- All voltages are referenced to Vcent
- All timing referenced to rising clock edge / strobe edges
- Mask is centered around Vcent and rising clock edge / strobe edges

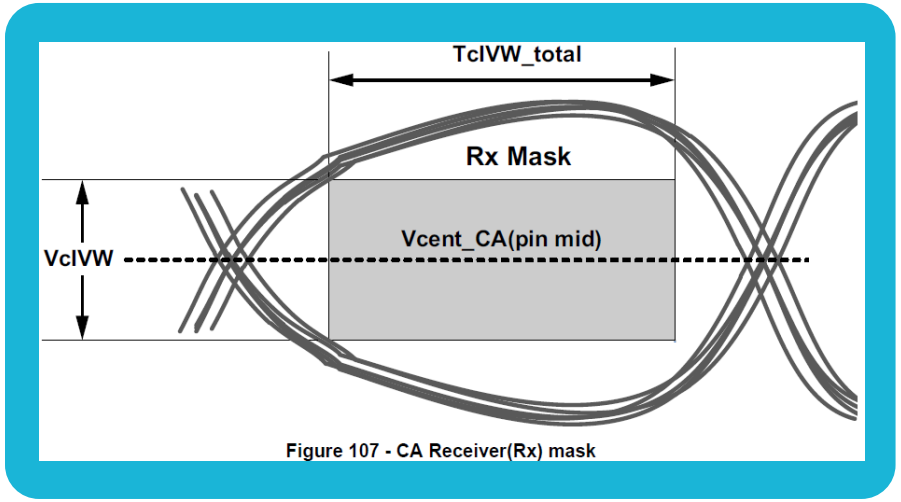


Figure 107 - CA Receiver(Rx) mask

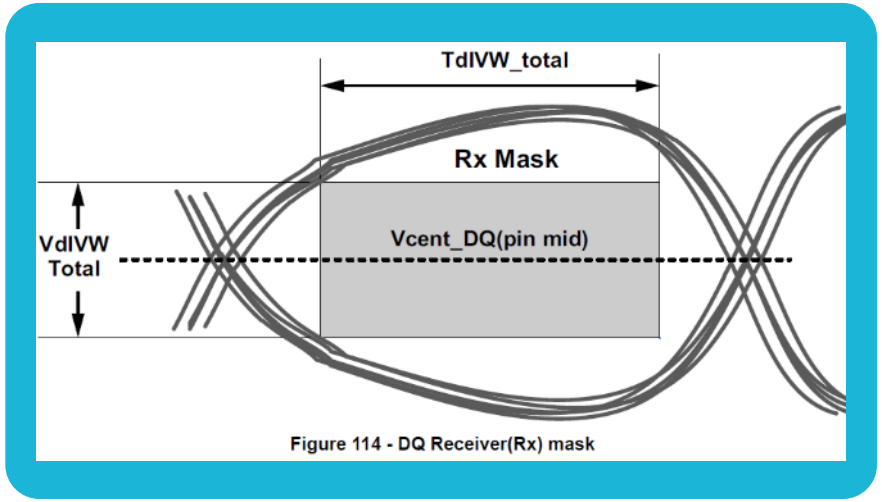


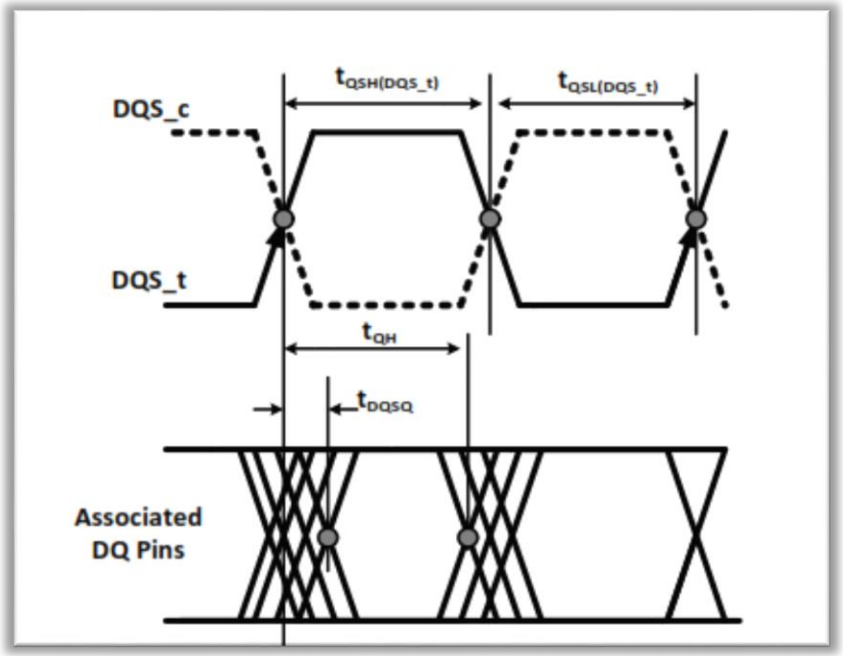
Figure 114 - DQ Receiver(Rx) mask

Conditions must be met cumulatively per group over time

Read / Write Timing

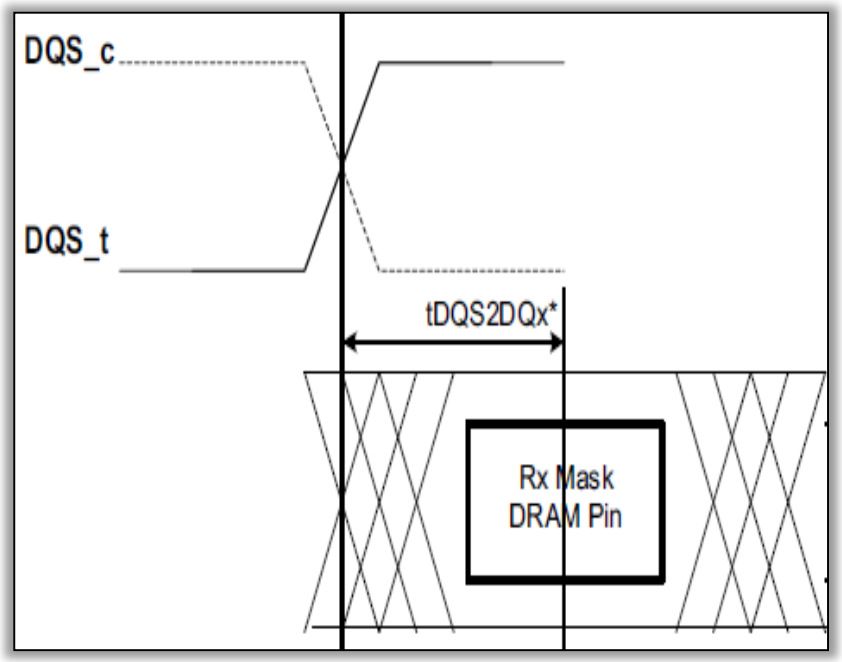
Read

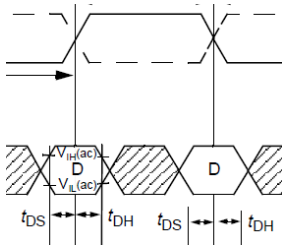
Data nominally EDGE aligned to strobe; similar to LPDDR2/3



Write

Data offset to strobe by tDQS2DQ; different from LPDDR2/3





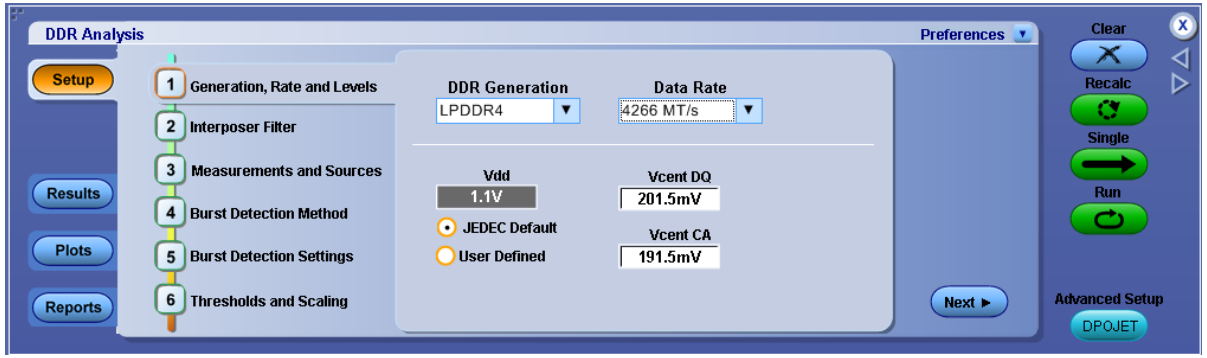
For reference:
LPDDR2/3: center aligned

LPDDR4 Compliance using DDRA

COMPREHENSIVE COVERAGE OF MULTIPLE JEDEC MEMORY STANDARDS IN A SINGLE PACKAGE

SUPPORT FOR ALL THE JEDEC DEFINED SPEED GRADES IN EACH STANDARD AS WELL CUSTOM SETTINGS

Memory Type	JEDEC Specification
DDR	JESD79E
DDR2	JESD79-2F
DDR3	JESD79- 3F
DDR3L	JESD79-3-1
DDR4	JESD79-4
LPDDR	JESD209A
LPDDR2	JESD209-2E
LPDDR3	JESD209-3
GDDR5	JESD212
LPDDR4	JESD209-4

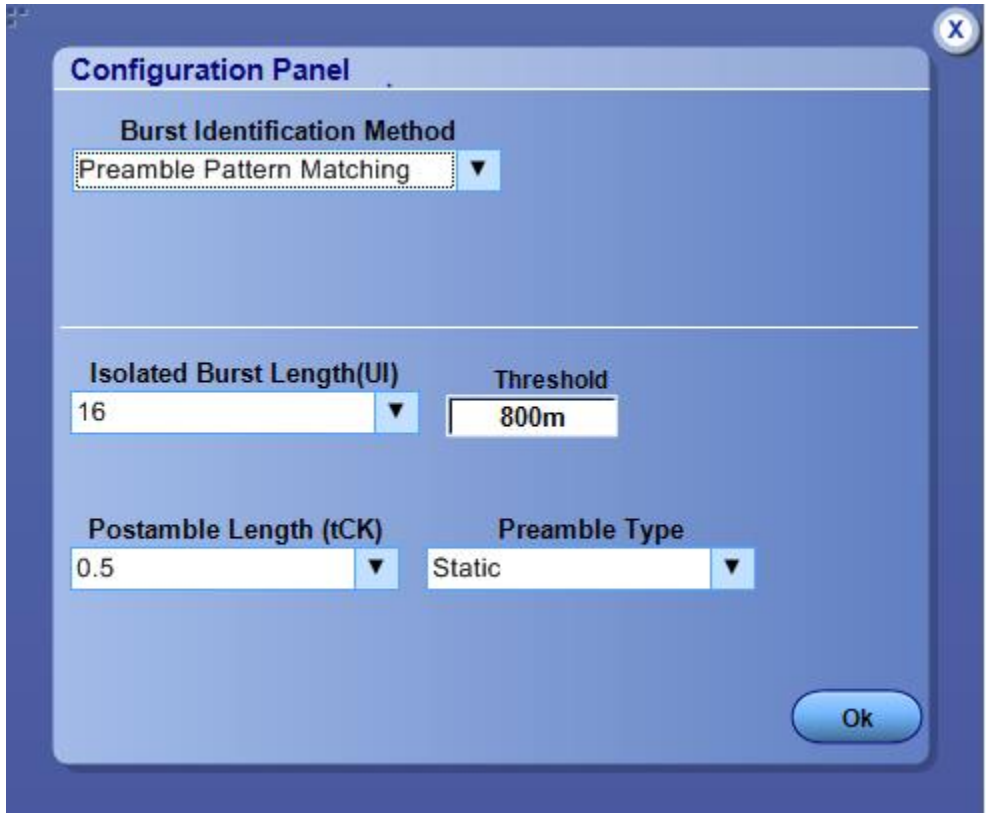


LPDDR4 Burst Detection

- ASM Algorithm : LPDDR4 has mainly two distinct differences compared to other DDRA generations.
  - Configurable Preamble type and Postamble length for the Read bursts.
  - No fixed phase relation between strobe (DQS) and data (DQ) in case of Write bursts. Instead there is a variable skew between DQS and DQ which can vary between 200ps to 800ps.
- Hence two new burst detection algorithms are introduced for LPDDR4 generation.
  - **Preamble Pattern Matching**
  - **Amplitude Based Burst Detection**
- One has to configure the burst detection parameters with the suitable values to get the right burst markings.

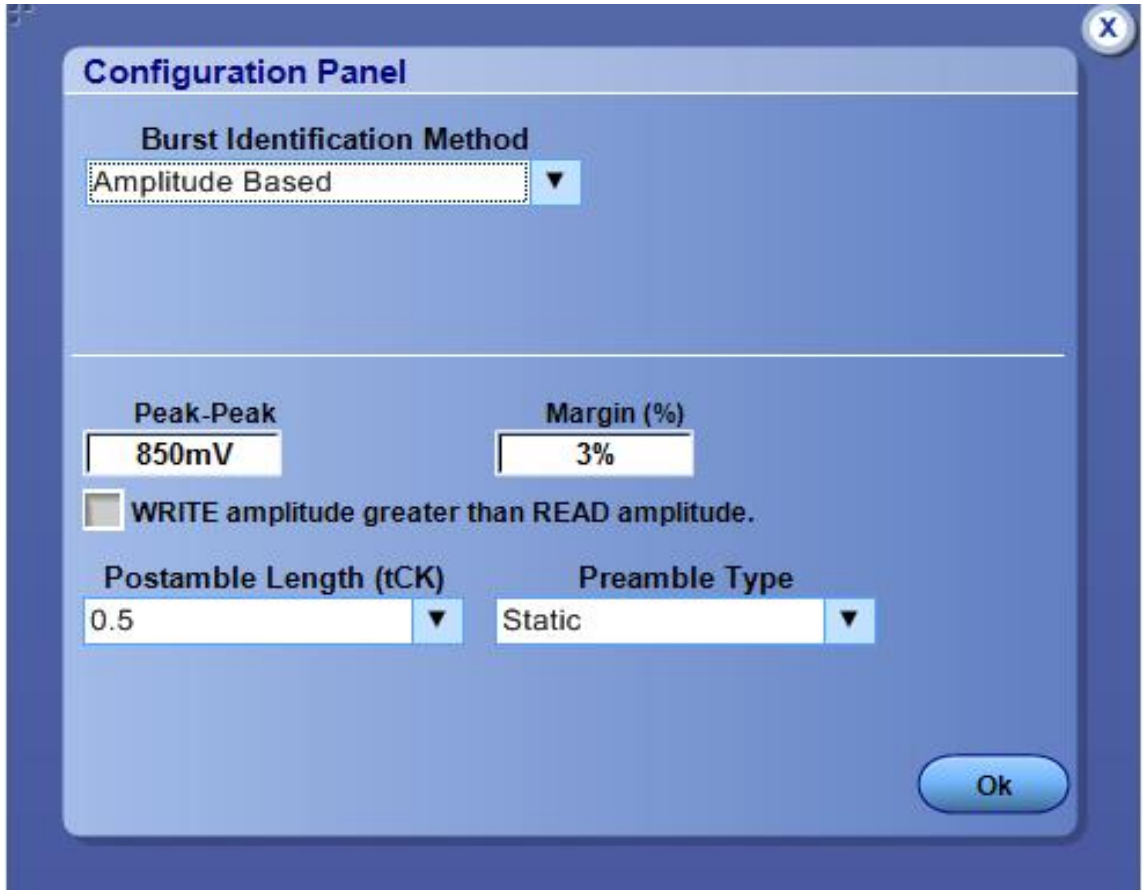
Preamble Pattern Matching

- **Isolated Burst Length:** Specify the isolated burst length with in the acquisition. For LPDDR4 it could be 16 or 32.
- **Threshold:** This parameter is a measure of similarity between READ or WRITE burst preamble. This value will range from 0 to 1. Note that this value is independent of the signal (strobe and data) amplitude.
- **Preamble Type:** Specify the READ burst preamble type as either ‘Static’ or ‘Toggle’.
- **Postamble Length:** Specify the READ burst postamble length. This could be either 0.5tCK or 1.5tCK (extended postamble).

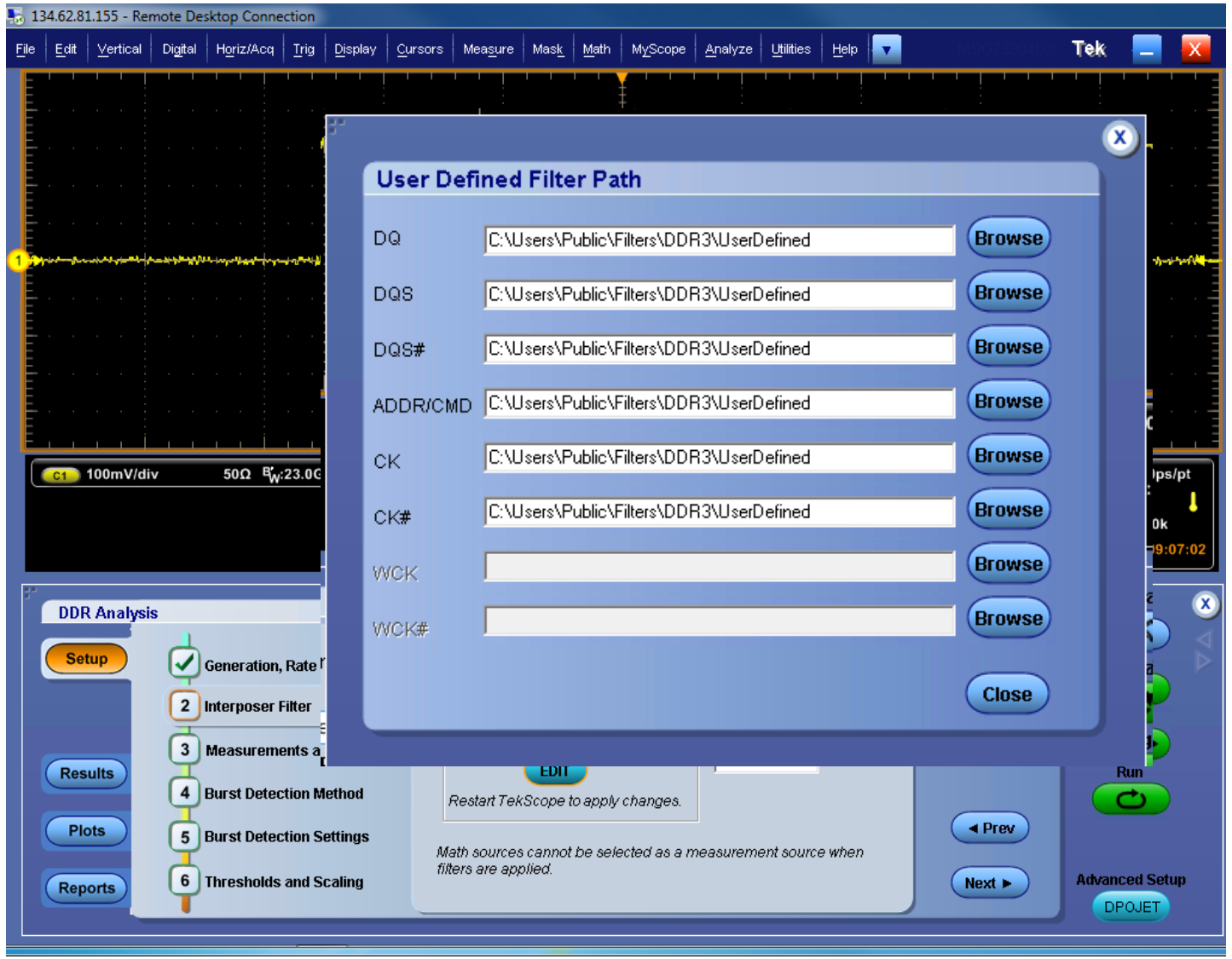


Amplitude based burst detection

- Select ‘Amplitude Based’ method when there is a considerable peak to peak voltage difference between READ and WRITE bursts.
- The algorithm detects the READ and WRITE bursts purely based on the burst amplitude.



Using Filters DDRA



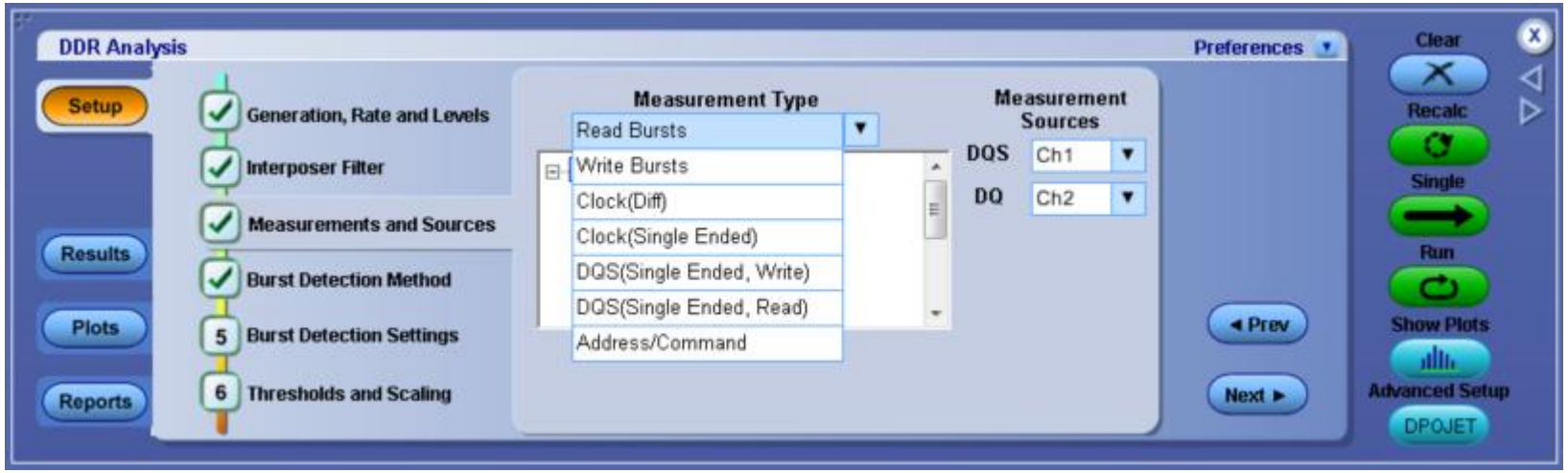
Test Setup and Configuration

- All the tests are logically grouped based on the input source requirement

  - READ, WRITE, CLOCK & ADDR/CMD

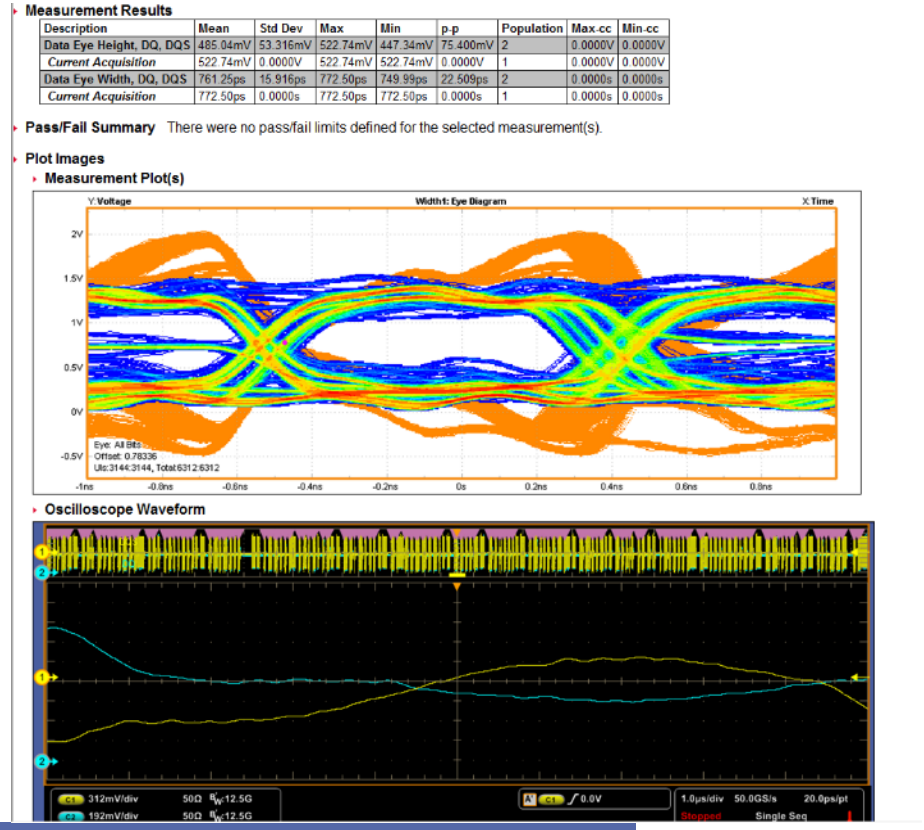
- Quickly set up the test configuration by selecting a complete group or individual tests for targeted analysis.

- Flexible input source requirement, inputs are not hardwired to a particular Oscilloscope channel.



Reports

- Analysis results are compiled into an HTML report enabling easy report management and distribution.
- Report includes
  - Measurement results
  - Pass/Fail test results based on specification values
  - Summary and detail plots
  - Oscilloscope screenshots
  - Measurement and Instrument configuration summary
- Report contents are user definable content
- Provision to append more results later



Measurement Results

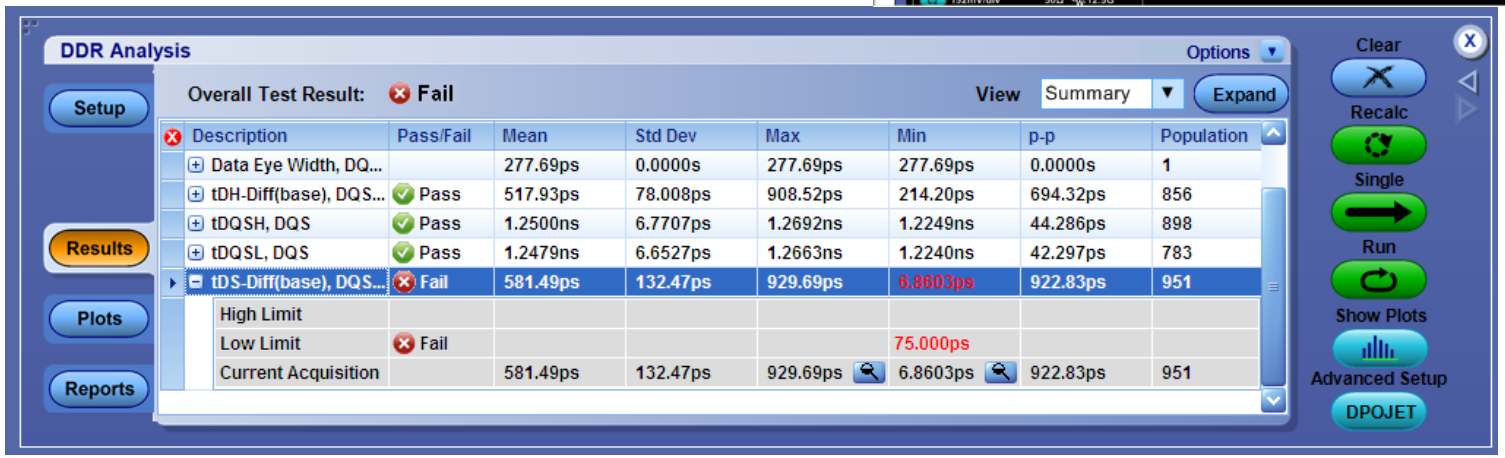
Description	Mean	Std Dev	Max	Min	p-p	Population	Max-cc	Min-cc
Data Eye Height, DQ, DQS	485.04mV	53.316mV	522.74mV	447.34mV	75.400mV	2	0.0000V	0.0000V
Current Acquisition	522.74mV	0.0000V	522.74mV	522.74mV	0.0000V	1	0.0000V	0.0000V
Data Eye Width, DQ, DQS	761.25ps	15.916ps	772.50ps	749.99ps	22.509ps	2	0.0000s	0.0000s
Current Acquisition	772.50ps	0.0000s	772.50ps	772.50ps	0.0000s	1	0.0000s	0.0000s

Pass/Fail Summary There were no pass/fail limits defined for the selected measurement(s).

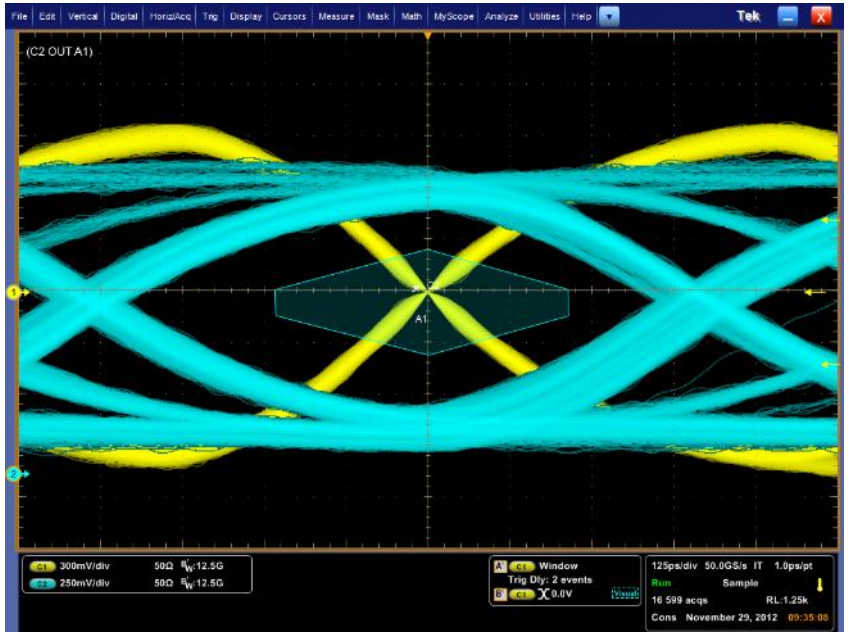
Plot Images

Measurement Plot(s)

Oscilloscope Waveform



Visual Trigger

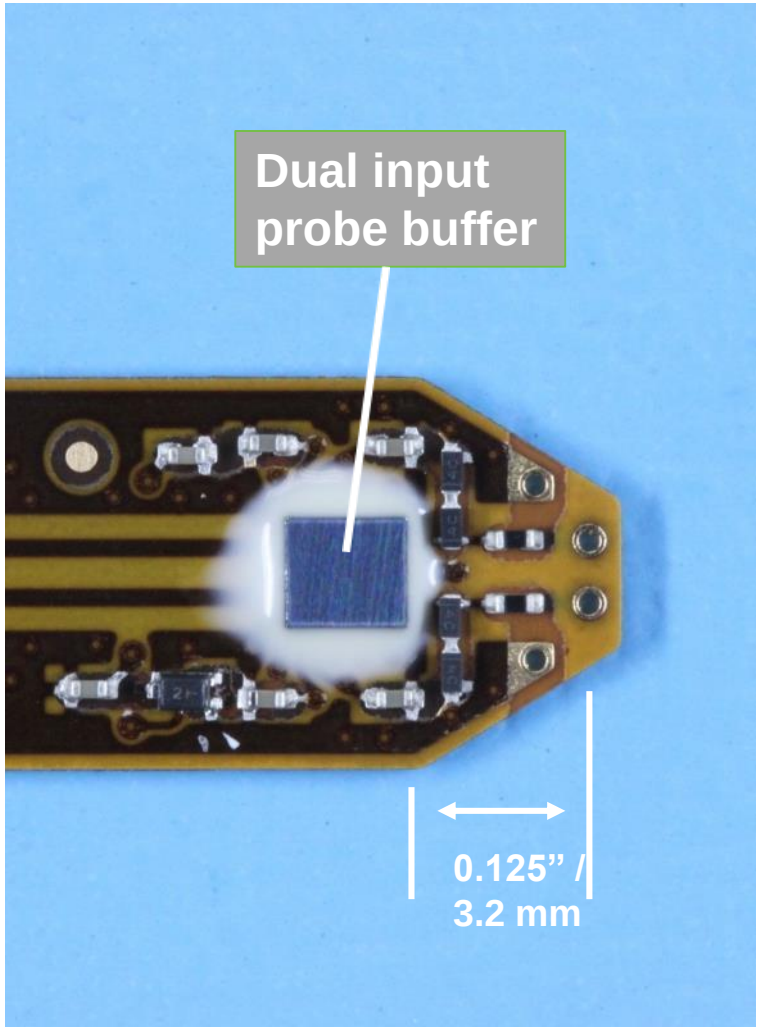


P7700 High Bandwidth TriMode™ Probe

- **NEW!** Active input directly at the probe tip
- **NEW**! TekFlex™ accessories
  - Improved access to tight test locations
- **Best-in-Class** low loading for
  - LPDDR and MIPI standards
- **Industry's lowest** cost per connection

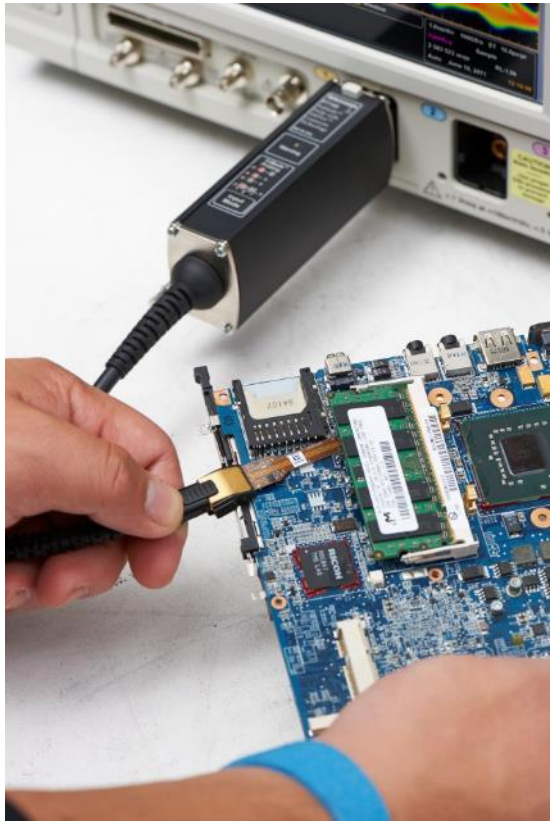
Probe Technology Innovations

- P7700 Offers the Industry's First "Chip-on-the-Tip"
  - Active input buffer on the solder tip
    - IBM's SiGe 8HP process
    - Minimizing signal loss, capacitance, and added noise
  - Probe tip amplifier less than 4 mm from the DUT connection



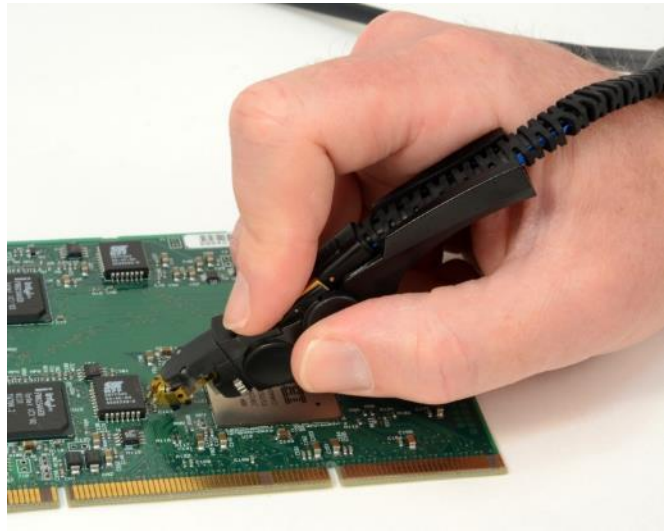
TekFlex™ Accessories

- Two Solder-in accessories with “Chip-on-the-Tip”
  - Flex circuit based and coax cable based tips
  - Up to 20 GHz bandwidth
  - TriMode functionality
    - Differential, single-ended, and common mode
  - Wide operative temperature range
    - -35°C to +85°C
- Industry leading usability and improved access to tight test locations
  - Flexible and Light
  - Easy to attach
  - Flat for ease of securing
    - Glue or tape used to relieve tension on solder connections



TekFlex™ Browser Accessory

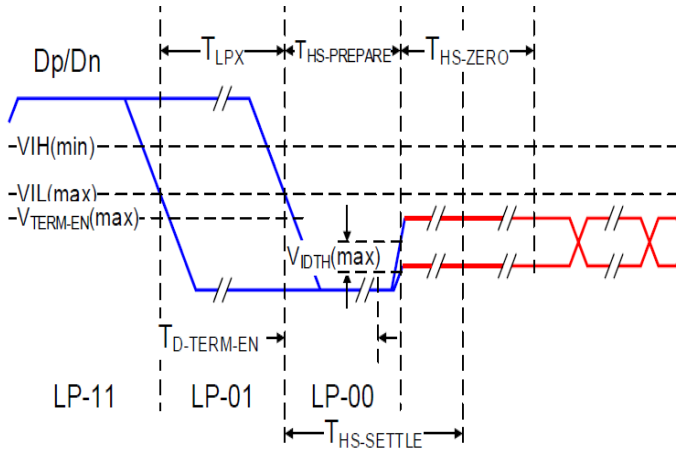
- Supports handheld and fixtured probing for multiple customer use cases
  - Debugging
  - Making quick measurements
  - Probing when a technician isn’t available for soldering
  - Checking power supplies and low frequency signals



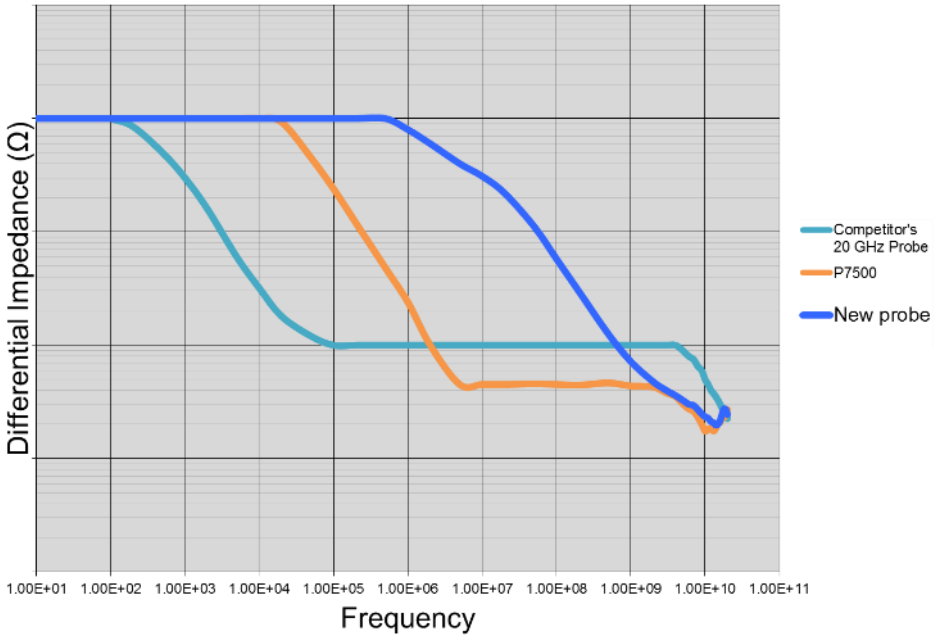
Best-in-Class Low Loading

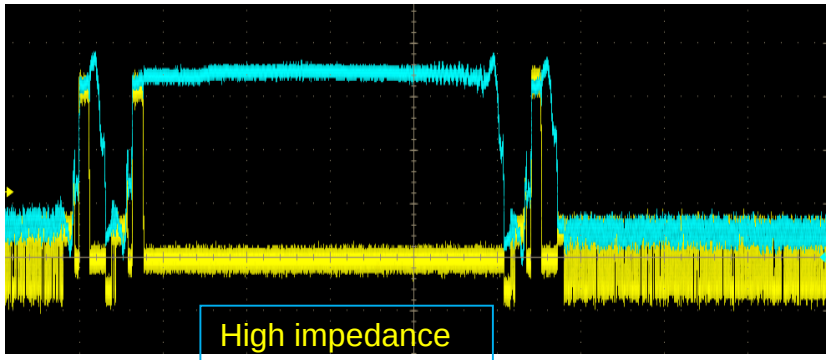
FOR LPDDR AND MIPI STANDARDS

- Mobile design goal is to maximize battery life in their designs
  - LPDDR and MIPI standards run unterminated to conserve power
  - Probe designed for high input impedance is required to limit LP bus loading



MIPI D-PHY HS Data Burst

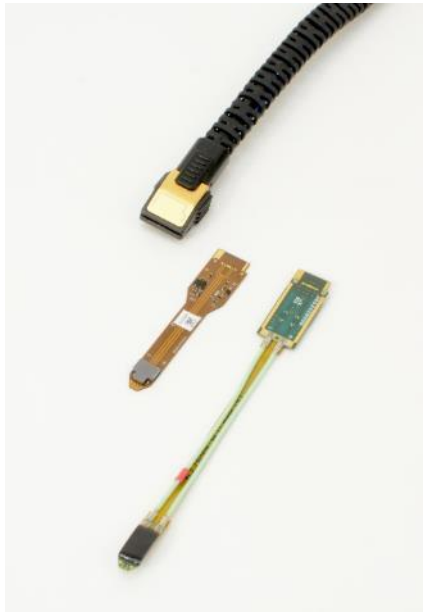




High impedance
Lower impedance

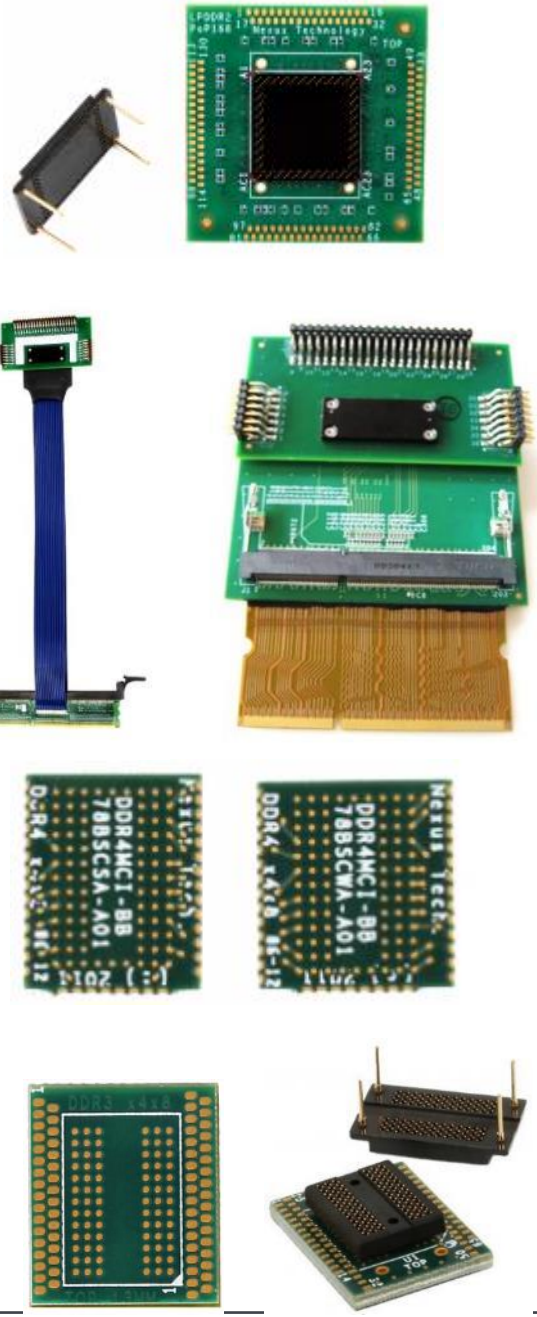
Lowering Overall Cost of Ownership

- Bringing probe and accessory costs down while increasing performance and user benefits
- Probe bandwidth is upgradable after purchase
- Lower cost per connection
  - ~$50 solder tip
  - Reusable ten times in typical use



Interposer Availability

Technology	Package / Form Factor
DDR2	Socketed – 60 Ball/ 84 Ball Solder-down – 60 Ball/ 84 Ball
DDR3	Socketed – 78 Ball/ 96 Ball Solder-down – 78 Ball/ 96 Ball Edge Probe – 78 Ball/ 96 Ball – Coming soon! DIMM Interposer for MSO SO-DIMM Interposer for MSO
DDR4	Socketed – 78 Ball/ 96 Ball Edge Probe – 78 Ball/ 96 Ball Edge Probe – 144 Ball – Coming soon! DIMM Interposer for MSO
LPDDR	Socketed – 60ball
LPDDR2	Socketed – 136 ball/168 ball/216 ball/240 ball
LPDDR3	Socketed – 216 ball Solder-down – 178 ball
LPDDR4	Socketed – 272 ball Edge Probe – 272 ball Solder-down – 200 Ball Solder-down – 366 Ball
GDDR5	Socketed – 170 ball Solder – down – 170 ball

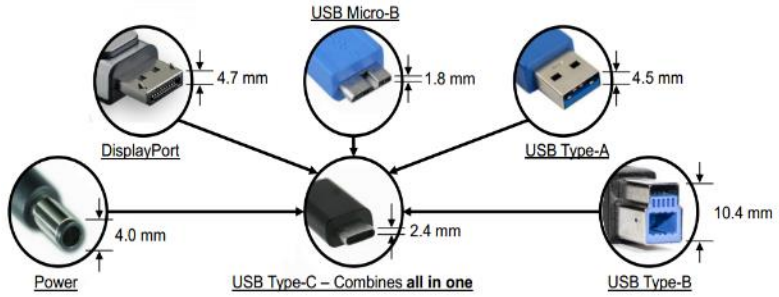


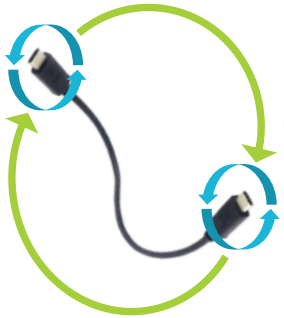
Tektronix LPDDR4 test solution

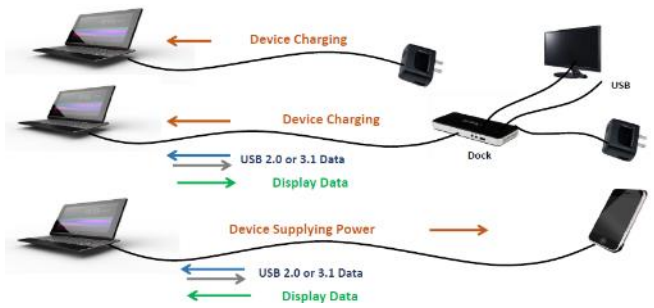
- √Provides easy access to signals through high performance interposers
- √Enables comprehensive LDDR4 interface JEDEC compliance using DDRA
- √The debug suite on the oscilloscope enables further analysis of LDDR4 waveforms for isolating an issue
- √Advanced Probing Solution

数据传输 - USB

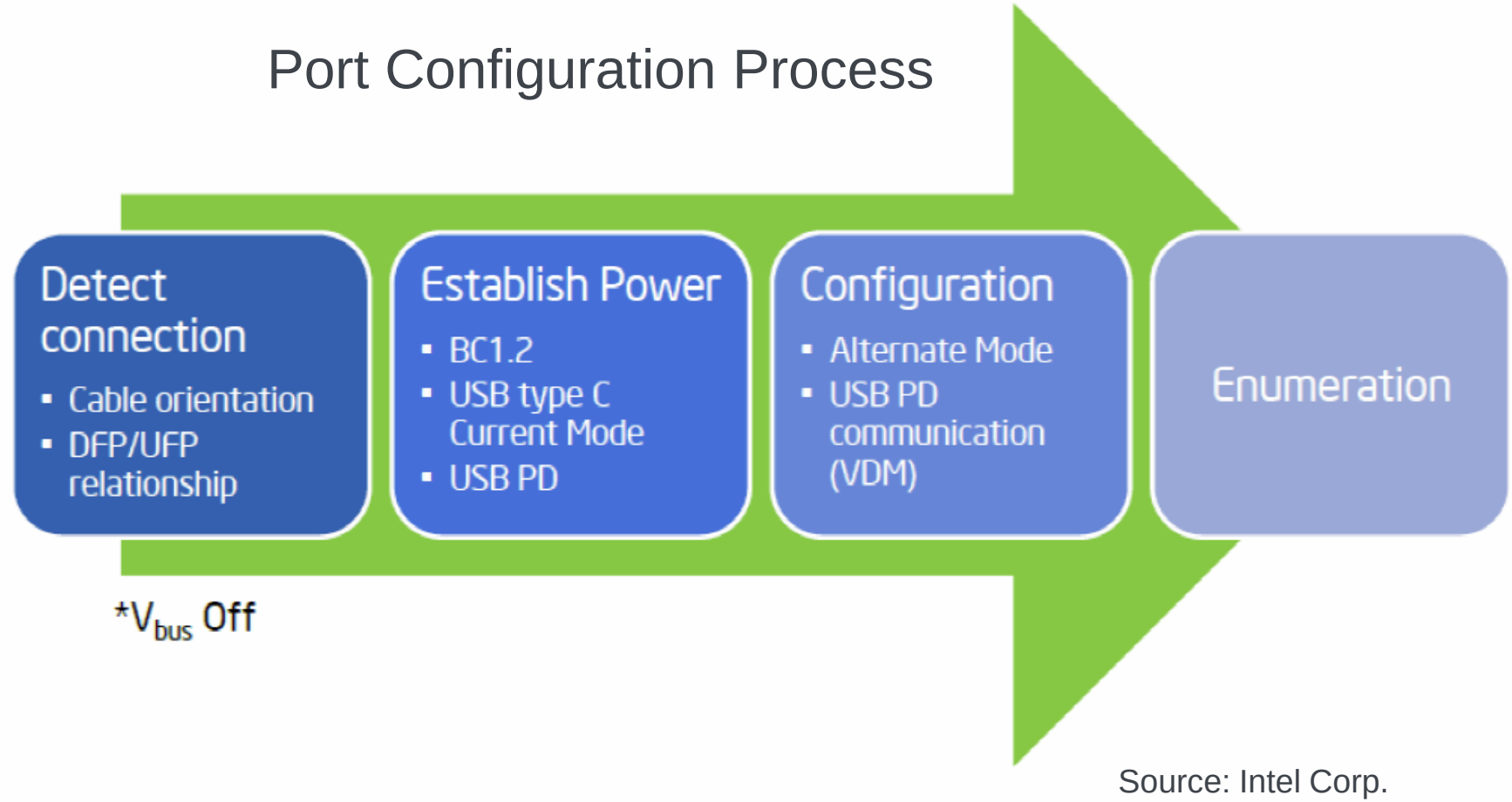
What is Type-C, why is it important?







USB = Data + Video + Power

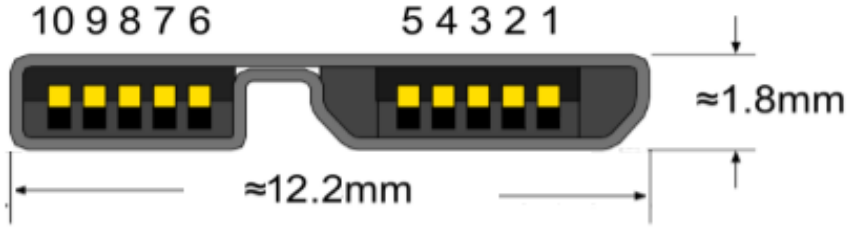


Source: Intel Corp.

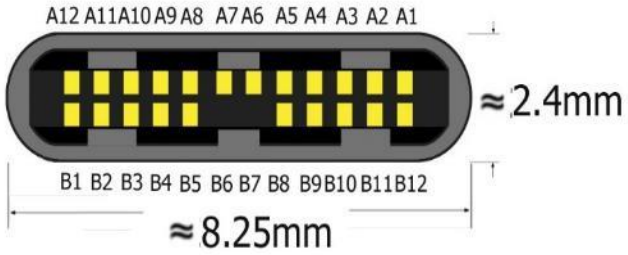
Type-C Comparison *(USB-C)*

- Rounded, reversible, flipable
- ~25% less width vs. µB
- Signaling
  - Two SS differential pairs
  - Vbus power
  - Configuration Channel (CC)
  - USB 2.0 differential pair
  - Sideband Use (SBU)
  - Plug power (Vconn)

Micro B Plug



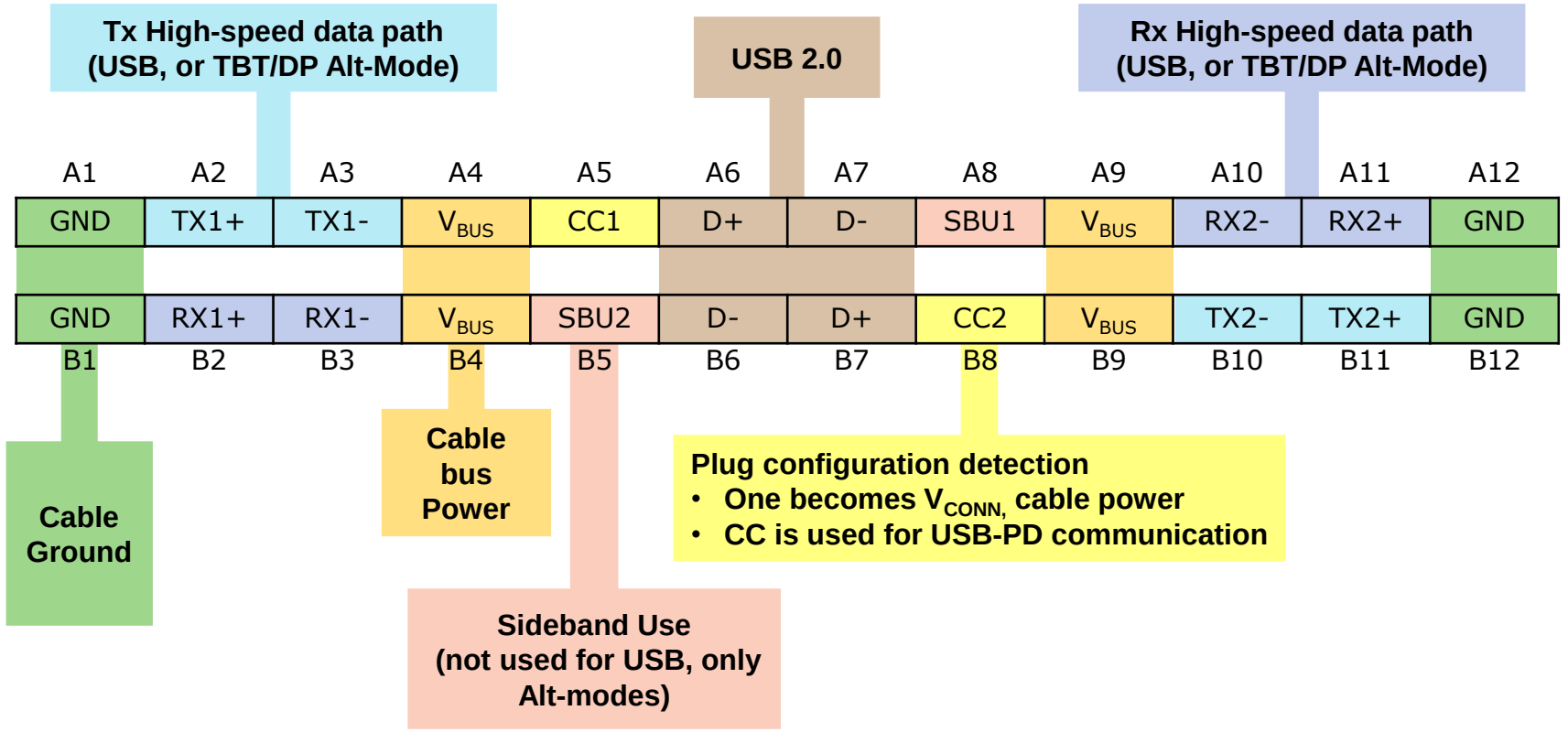
Type-C Plug



* New signals

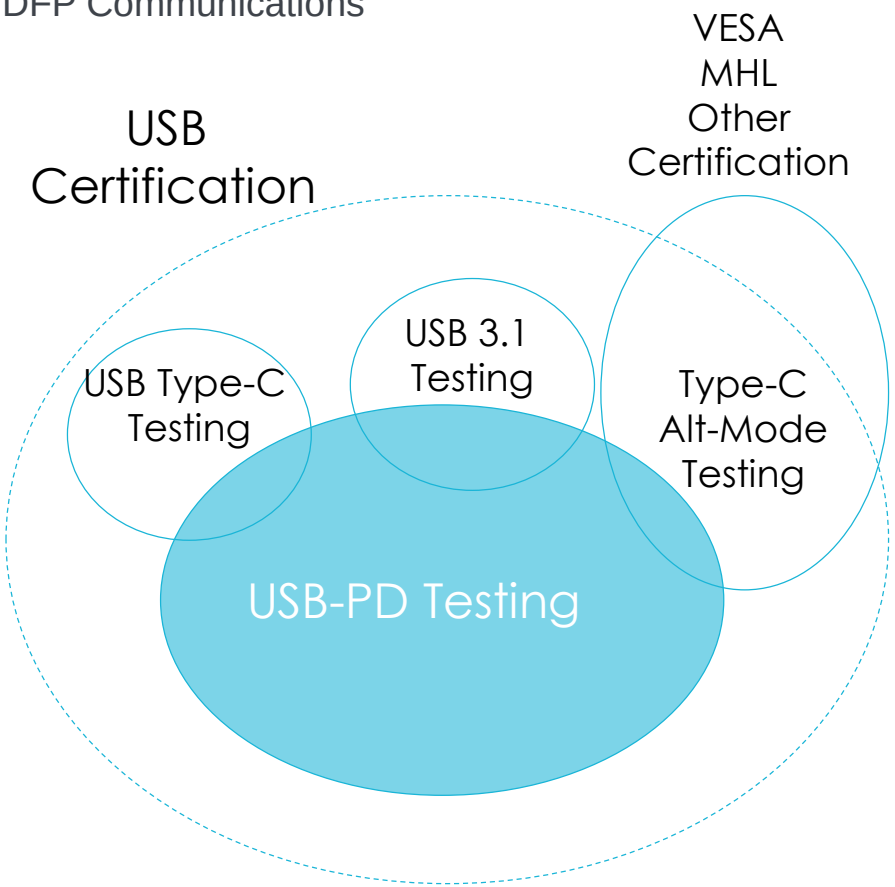
A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
GND	TX1+	TX1-	VBUS	CC	D+	D-	SBU1	VBUS	RX2-	RX2+	GND
GND	RX1+	RX1-	VBUS	SBU2			VCONN	VBUS	TX2-	TX2+	GND
B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1

Type-C Pin Definitions

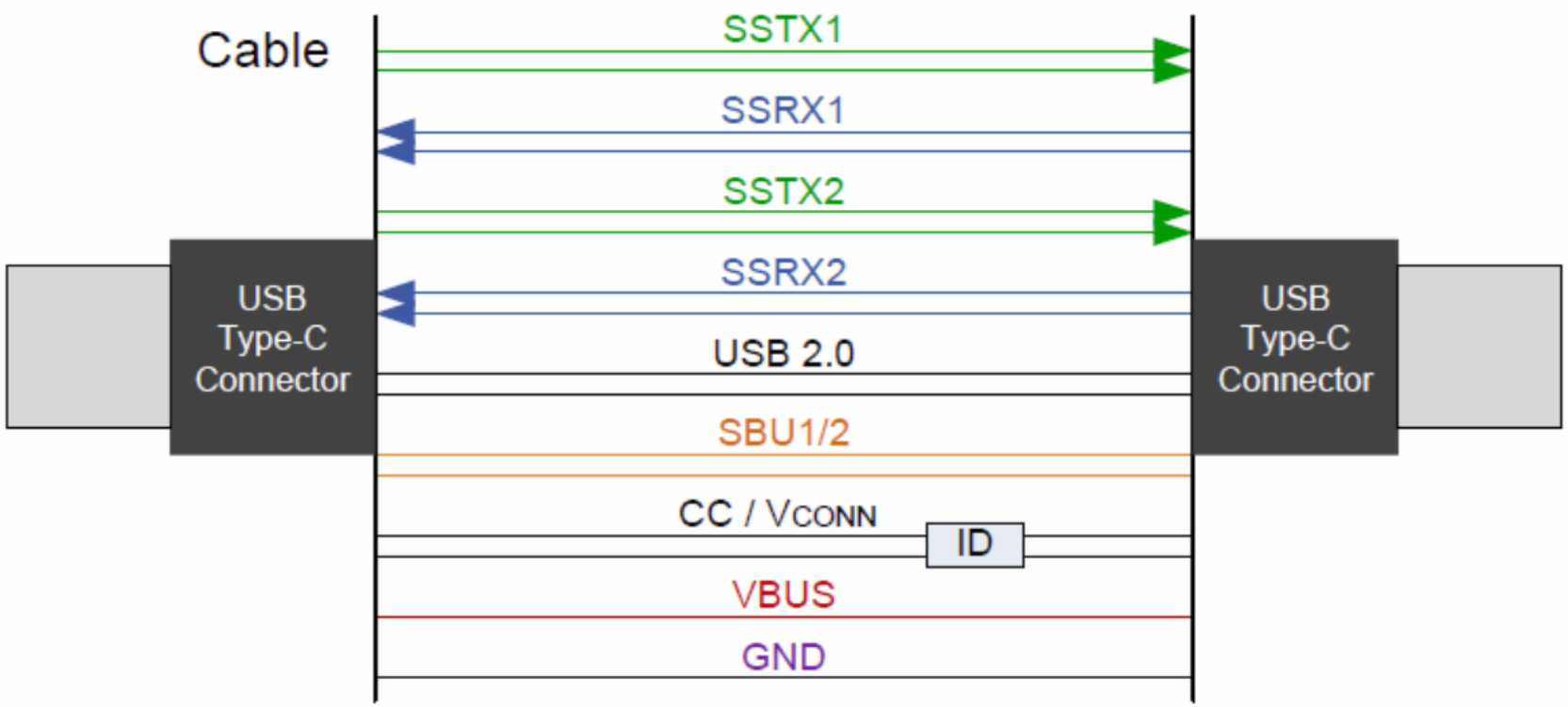


USB-PD & DisplayPort Specification & CTS Overlap

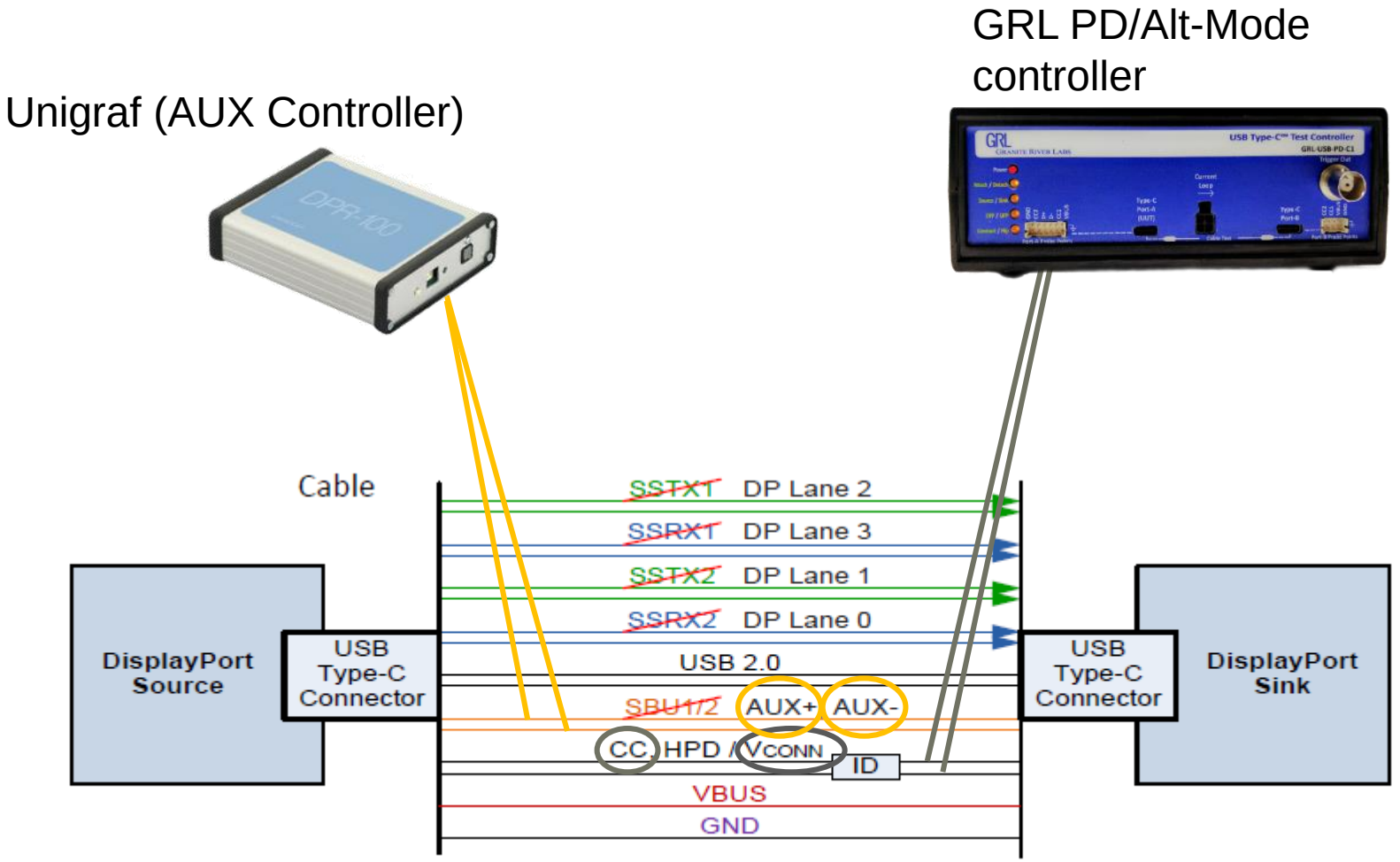
- USB Power Delivery Rev2.0, V2.0
  - Chapter 2 - Overview Section including SOP* Comm and UFP/DFP Communications
  - Chapter 3 Type-A and TypeB Cable Assemblies & Connectors
  - Chaper 4 Electrical Requirements
  - Chapter 5 Physical Layer (BMC & FSK)
  - Chapter 6 Protocol Layer
  - Chapter 7 Power Supply
  - Chapter 8 Device Policy
  - Chapter 9 System Policy
- USB Type-C Cable Specification Rev1.0
  - Chapter 4 – Type-C Functional Testing
- DisplayPort Alt Mode on USB Type-C
  - Chapter 5 – Discovery and USB-PD
- TBT and other ‘Alt Modes’



USB 3.1 Data Mode

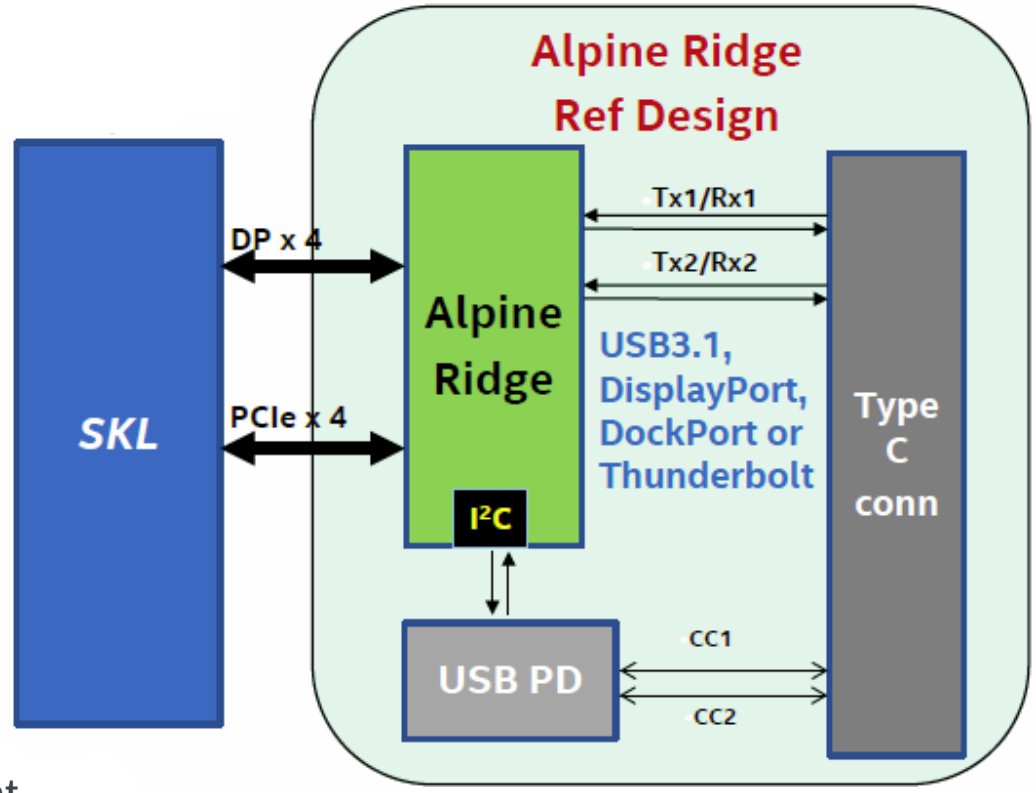


DisplayPort Mode (Alt mode)



Thunderbolt Mode

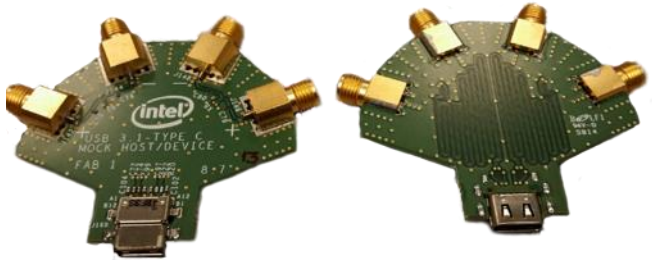
- Integrate Type-C solution (Alpine Ridge)
- Targeted for Intel Skylake platform
- Key features
  - Native USB 3.1 (10 Gb/s)
  - DP over Type-C (4K Video)
  - Thunderbolt (20 Gb/s)
  - DockPort
- Tektronix to provide full Alpine Ridge support in Q3 2016
  - TBT3 controller automation with 4x faster 10G/20G measurement automation
  - Use new TBT 20G Type-C fixture



Test Fixtures

- USB 3.1 fixtures
  - **USB-IF** (required for certification)
    - ❖Type-C, Standard/Micro A/B
    - ❖Includes USB-specific channels
    - ❖Available **now** on USBIF website!
  - **Wilder Technologies**
    - ❖DP Type-C fixtures also work for USB
  - **Luxshare-ICT**
- DP over Type-C
  - **Wilder Technologies**
  - **Luxshare-ICT**

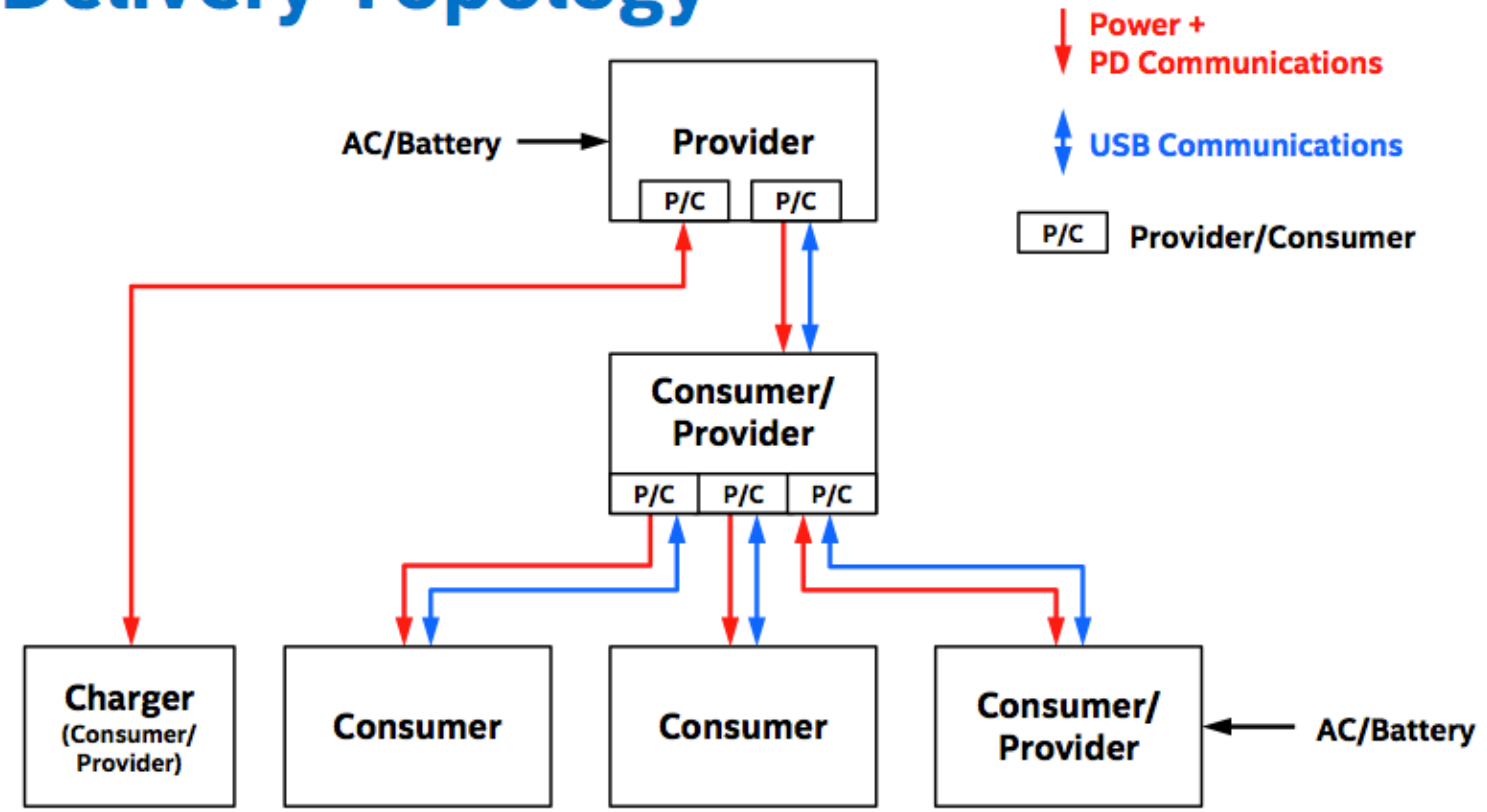
USB-IF
Type-C Fixtures & Channels



Luxshare-ICT
High Speed Plug Fixture

Wilder DP Fixture

Power Delivery Topology



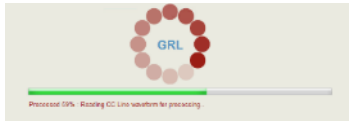
Run Tests

Scope Acquisition

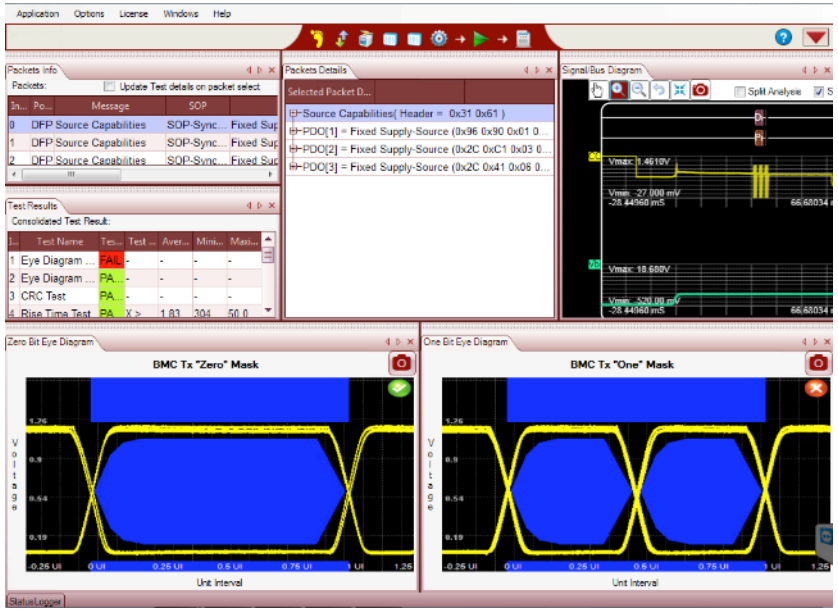
Useful Scope Features

- Lowest Analog BW (100-200MHz)
- High Res Acquisition Mode to filter noise
- Pulse Width Trigger
- Segmented Memory
- Desired: CC Packet Trigger
- HF Reject Trigger Coupling

Press Run



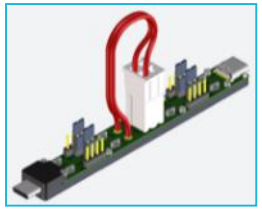
Results ‘Dashboard’

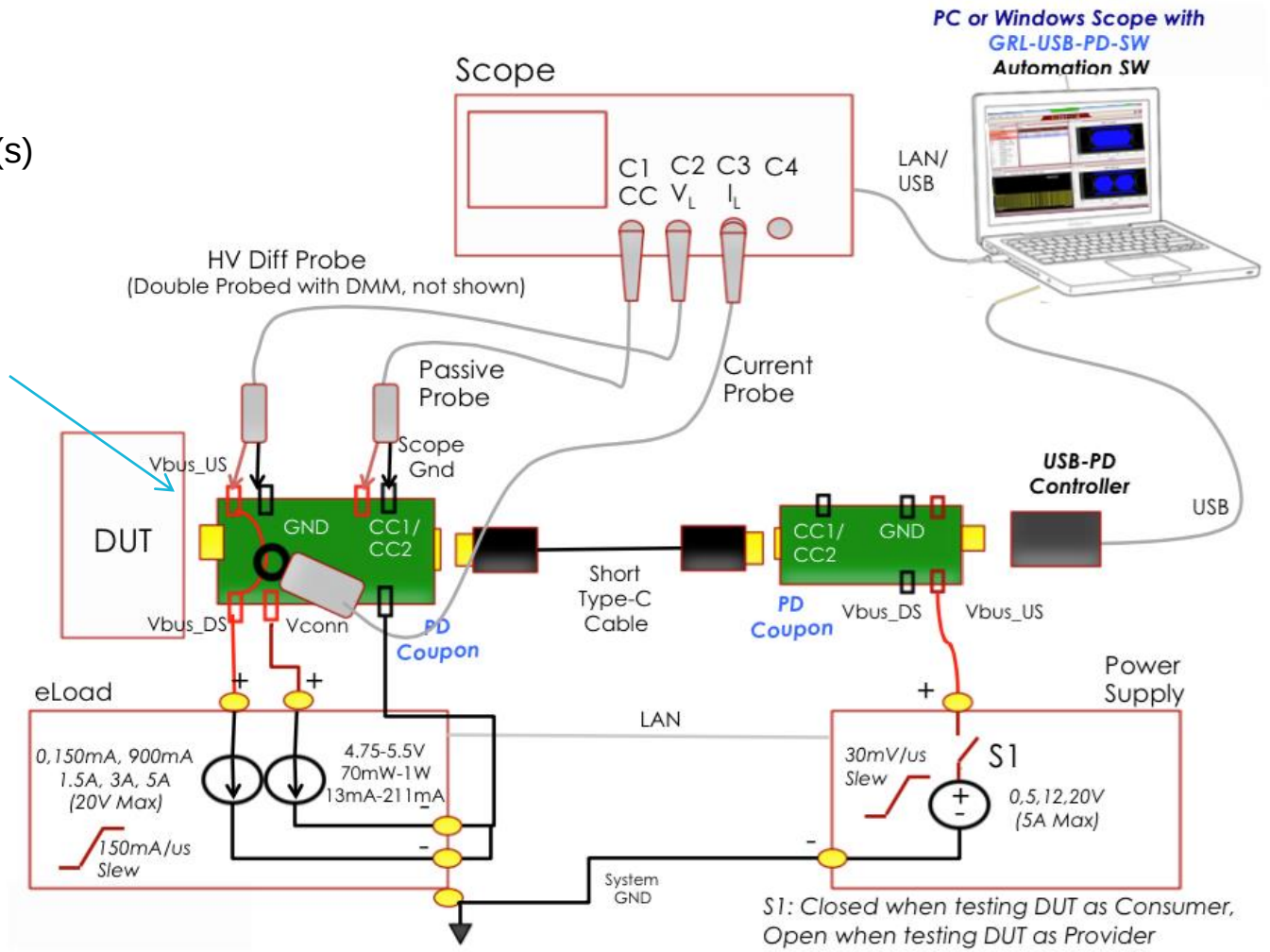


GRL-USB-PD Software

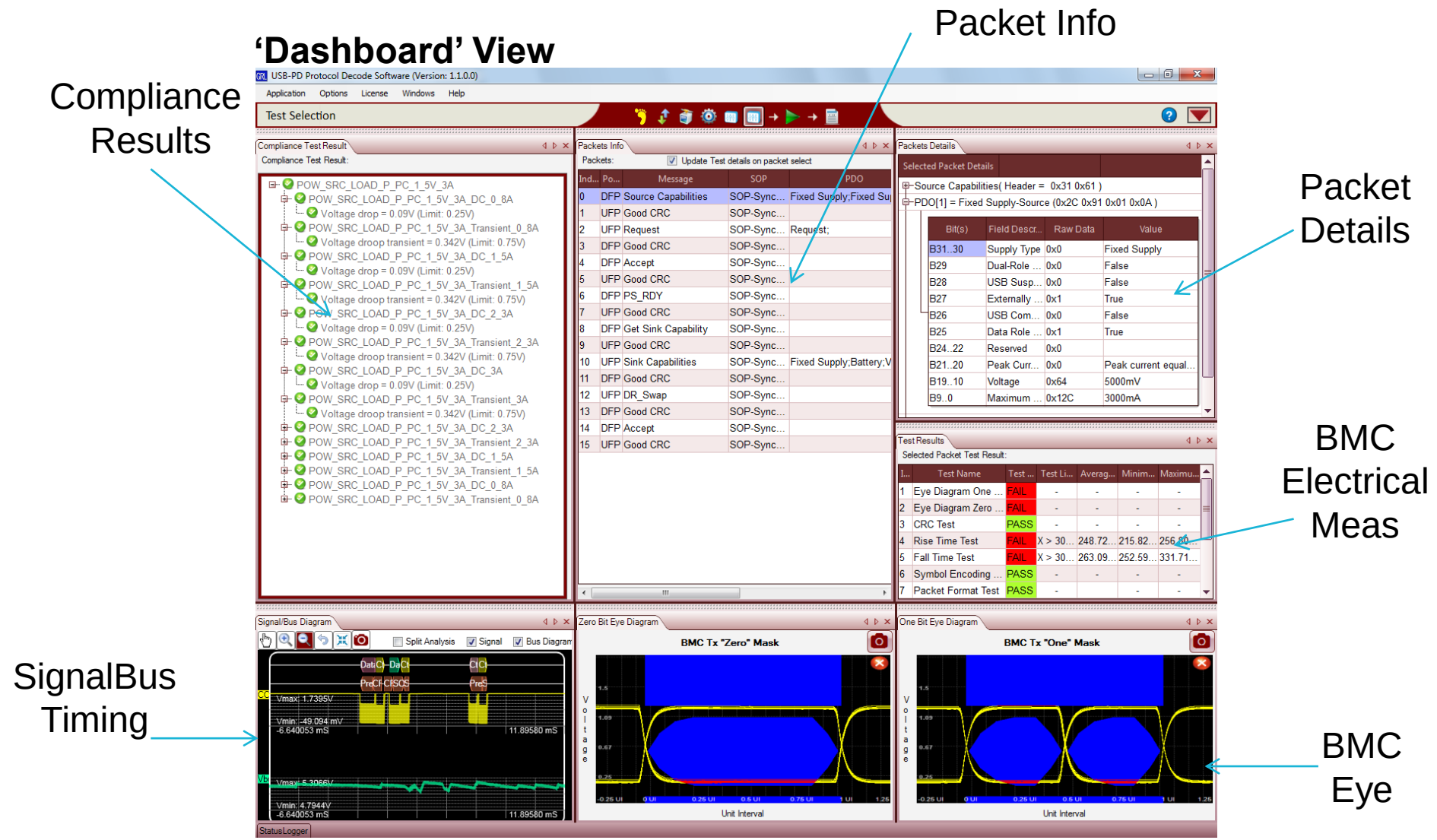
Confirm Test Setup (Provider/Consumer Example)

USB-PD Coupon(s)





View Test Results



Complete USB-PD Compliance Solution

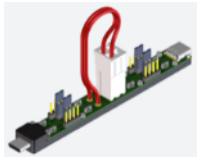
- **Required Equipment for PD Testing**
  - Order Oscilloscope from Tektronix
    - ❖**DPO5000 Series** Scopes and above
    - ❖**GRL-USB-PD** Power Delivery SW
    - ❖**2ea. Passive Probes** for CC and VBUS
    - ❖**1ea. TCP-2020A Current Probe** for Load Current
  - Order USB-PD Controller from GRL
    - ❖**1 ea. GRL-USB-PD-C1** Controller
  - Keithley eLoad & Power Supplies:
    - ❖**1 ea** – **Keithley 2380** DC E-Load
    - ❖**Optional Lab PS** – **Keithley 2280S-32-6** (32V/6A)
  - Download Data Sheet and Demo SW, MOI
    - ❖www.graniteriverlabs.com/usb-pd/

TekScope

TCP-2020A

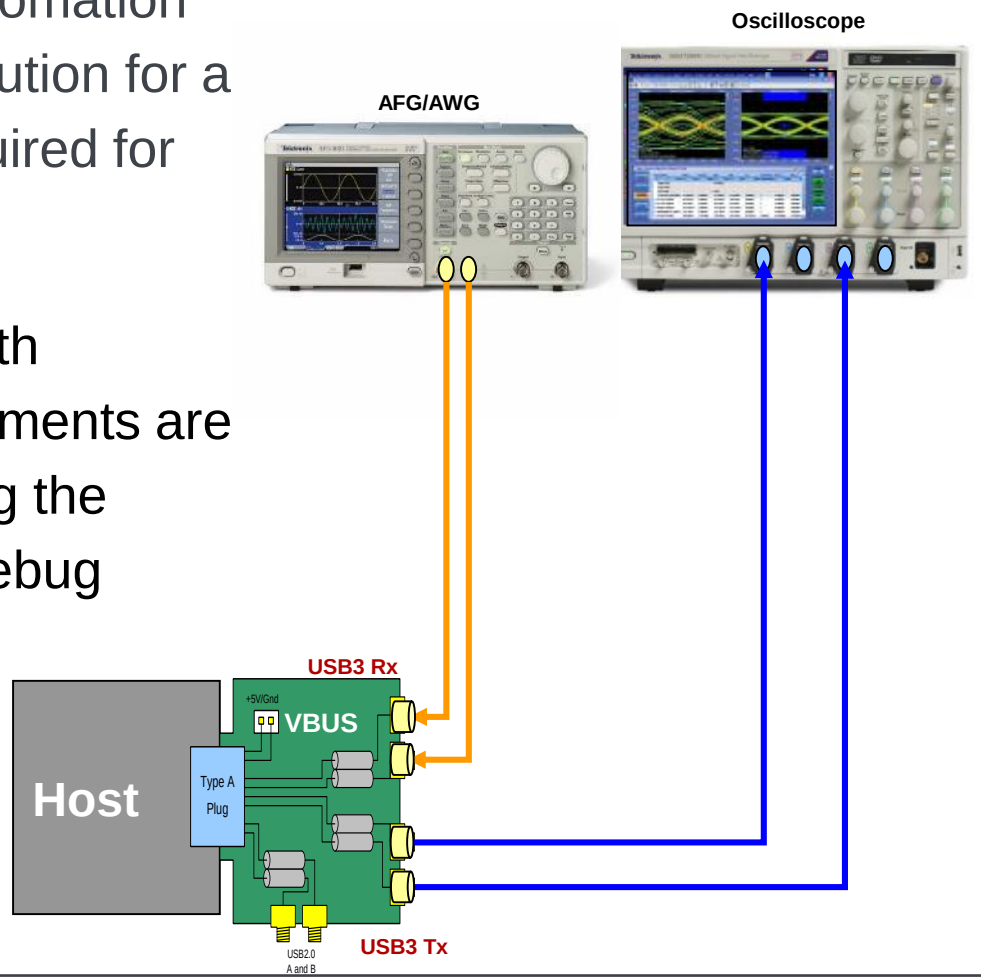
Keithley 2380

GRL-USB-PD-C1



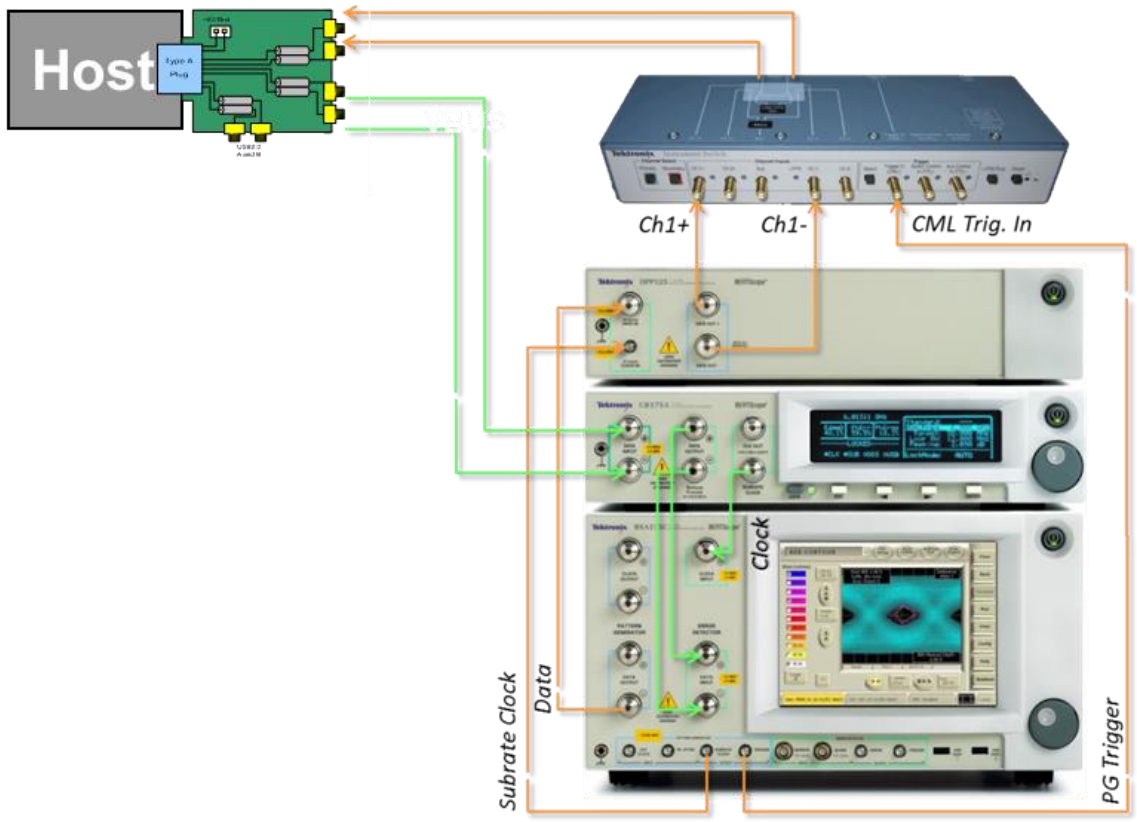
USB 3.1 Transmitter test

- Tektronix offers test efficiency, automation capability, and a simple to use solution for a wide range of measurements required for USB 3.1 certification.
- In addition to automated tesing with TekExpress, all USB 3.1 Measurements are implemented in DPOJET providing the engineer with a comprehensive debug environment

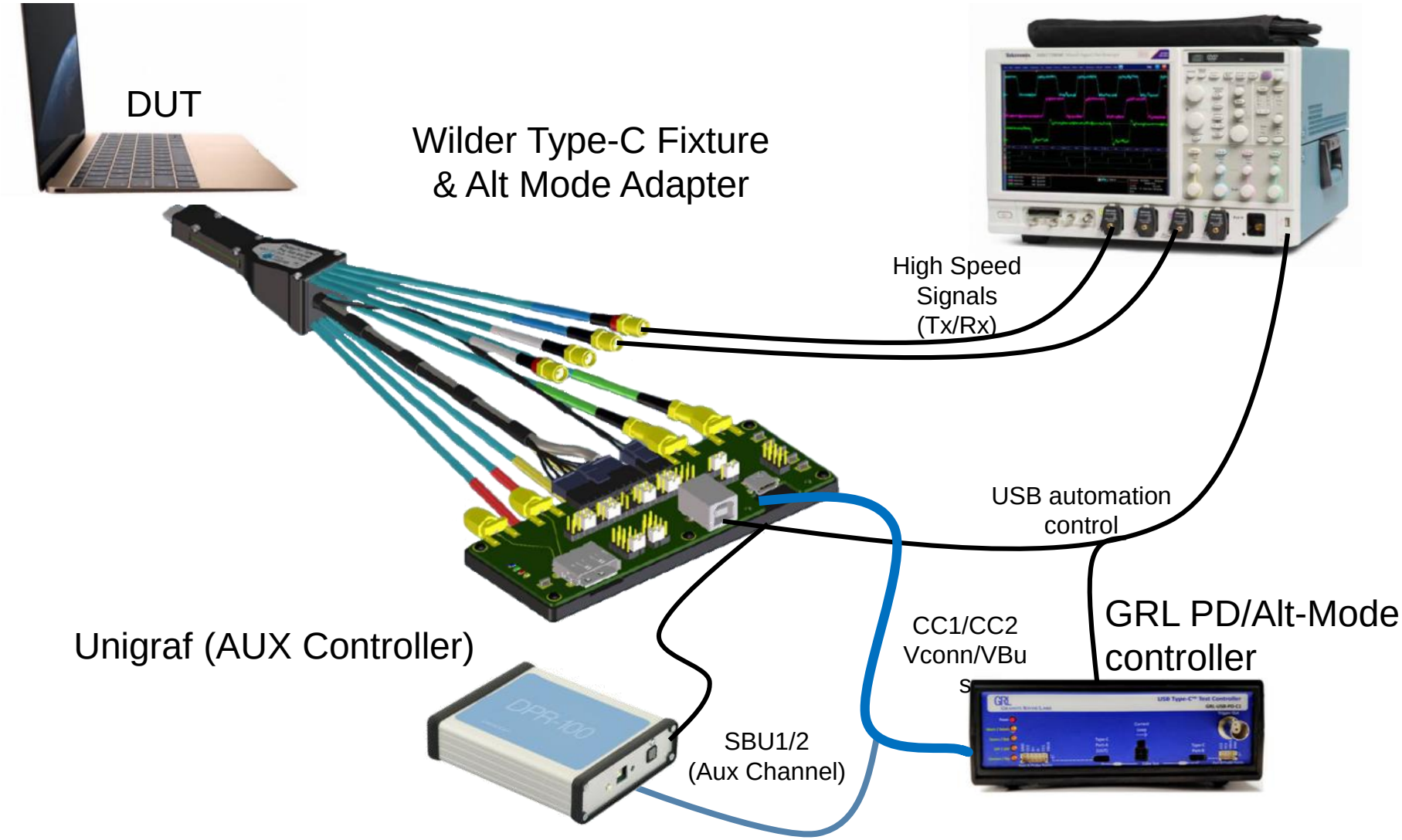


USB 3.1 Receiver test

- The BERTScope allows customers to define custom SSC profiles, bit rates, and accurate de-emphasis settings
- BERTScope-based USB3.1 solution includes flexible loopback controls and user-defined margin analysis



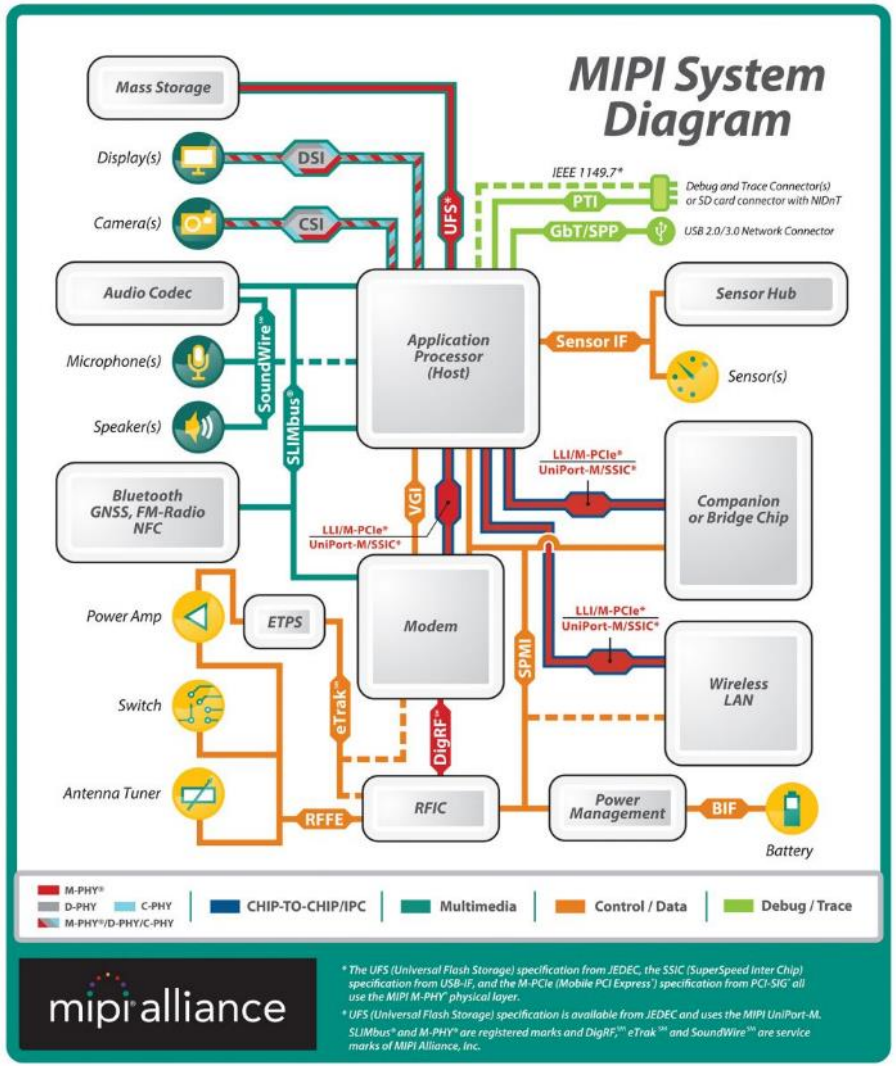
Tektronix DP Type-C solution



Tektronix is the only company that provides an integrated debug solution to enable finding root causes for signal integrity problems

数据传输 - MIPI

MIPI Overview



MIPI PHY	M-PHY	D-PHY	C-PHY
Applications	Storage Devices, Modem Chips, RFIC, Companion chip	Camera & Display	Camera & Display
Protocols	UniPro, UFS, SSIC, MPCIe	CSI-2, DSI-1	CSI-2, DSI-1
Clocking	Embedded	Source Synchronous, SSC	Embedded
Channel Compensation	Equalization	Data skew control relative to clock	Encoding to reduce data toggle rate
Signaling	NRZ for High Speed, Distinct PWM mode for Low Power	NRZ , Dynamic LP-HS Transition	3-level signaling over 3 wires, Dynamic LP-HS Transition
Minimum Pins	2 (Data)	4 (2 Data + 2 Clock)	3 (Data)
High Speed Data Rate	1.5Gb/s to 11.6Gb/s	500Mb/s - 4.5Gb/s	3GS/s
Encoding	8b10b	8b9b	16 bit to 7 Symbol

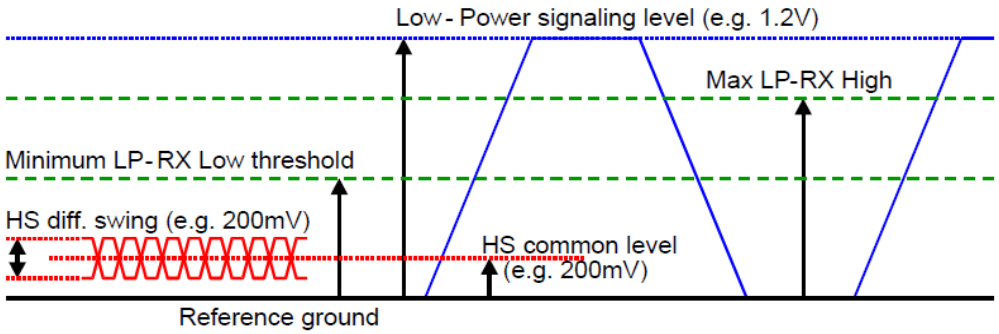
MIPI Measurement Challenges Overview

MIPI OVERVIEW

- Signal access
- Complex signaling
- Tests specified at RX or TX pin
- Terminated and un-terminated modes
- Differential and non-differential signaling
- Low power (LP) and high-speed (HS) modes
- Switchable termination networks
- Receiver stress dependencies
- New measurements required
- Multi-lane testing
- Different encoding schemes
- Different clocking architecture
- Built-in chip/SoC error detectors

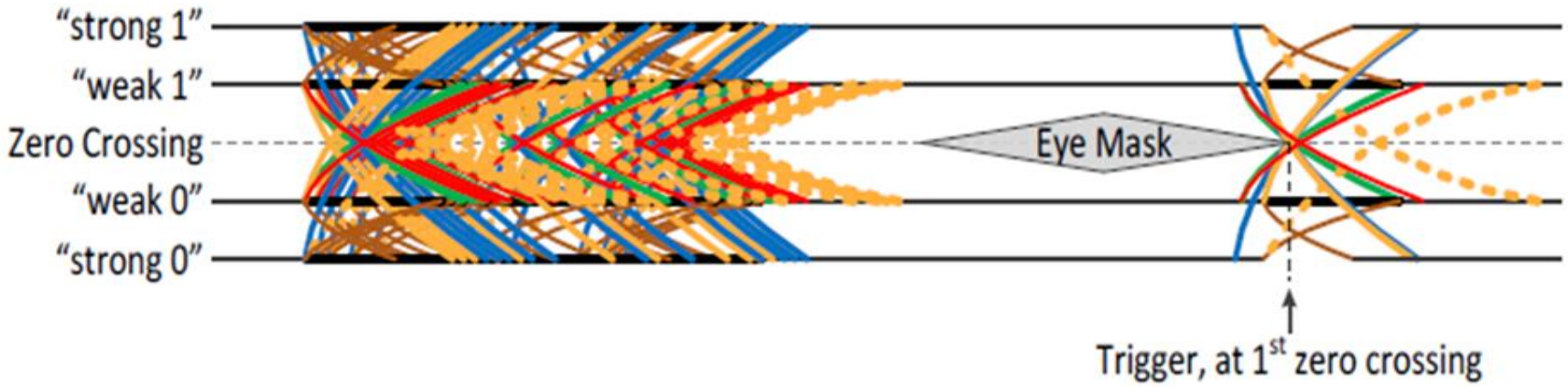
D-PHY Challenges

- D-PHY v2.0 specifies bit rates up to 4.5Gb/s
- Separate measurement specs for LP and HS modes.
- Receiver stress includes clk-data skew, common mode (CM) and differential mode voltage, eSpike and Tmin-rx events, and CM noise interference
- Error detection using on-chip/SoC error detector
- Channel ISI may minimized by TX pre-emphasis
- TX and RX input impedance tolerance



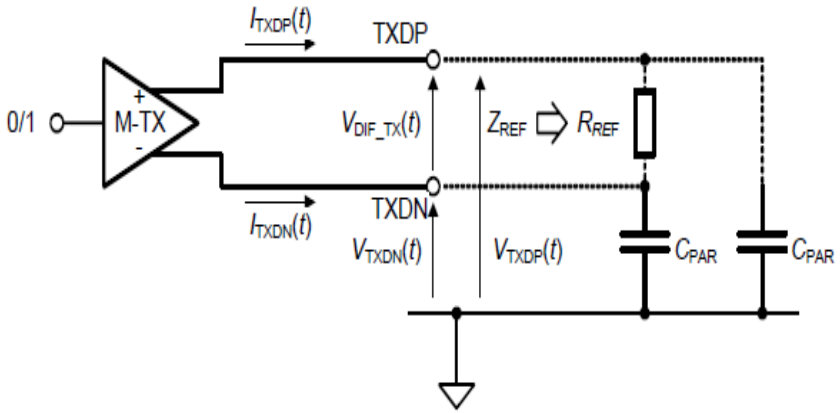
C-PHY Challenges

- C-PHY v1.0 specifies bit rates up to 2.5Gbaud/s, an aggregate bit rate over three-wire lane of 5.7Gb/s
- Separate measurement specs for LP and HS modes.
- TX measurements rely on 1st triggered edge clock recovery
- Receiver stress includes slew rate, channel ISI, CM and differential mode voltage and duty cycle distortion
- TX and RX input impedance tolerance

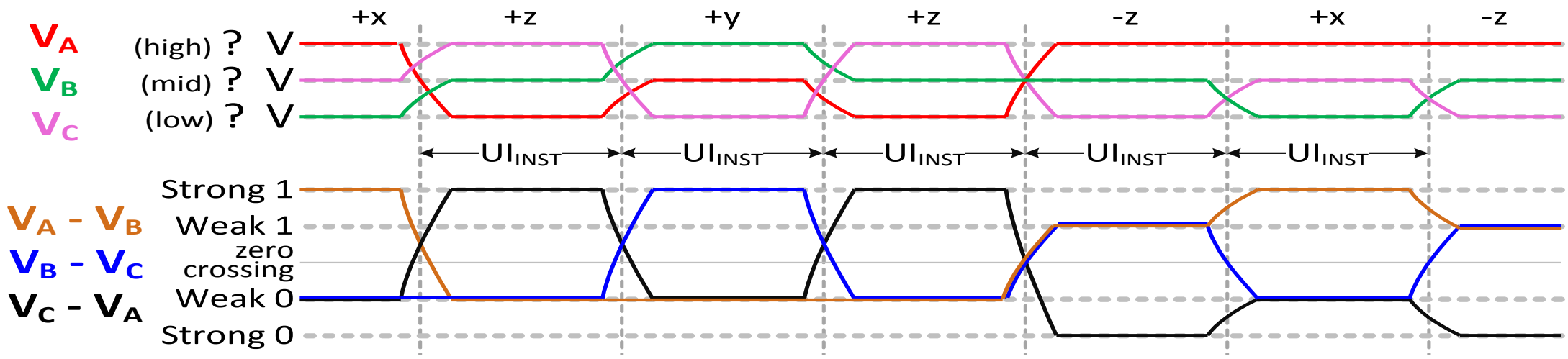


M-PHY Challenges

- M-PHY v3.1 specifies bit rates up to 5.83Gb/s, with a roadmap to support >10Gb/s signaling in future.
- Separate measurement specs for LP and HS mode
- Multiple bit rates for LP and HS.
- Requirement to separate jitter and noise, extrapolate eye openings to 1E-10 for transmitter testing
- Receiver stress includes ISI, CM and differential mode voltage, Rj & Sj
- Stress calibration critical to margin and jitter tolerance
- TX and RX input impedance tolerance – 100 Ohms for HS and NT for LP Mode



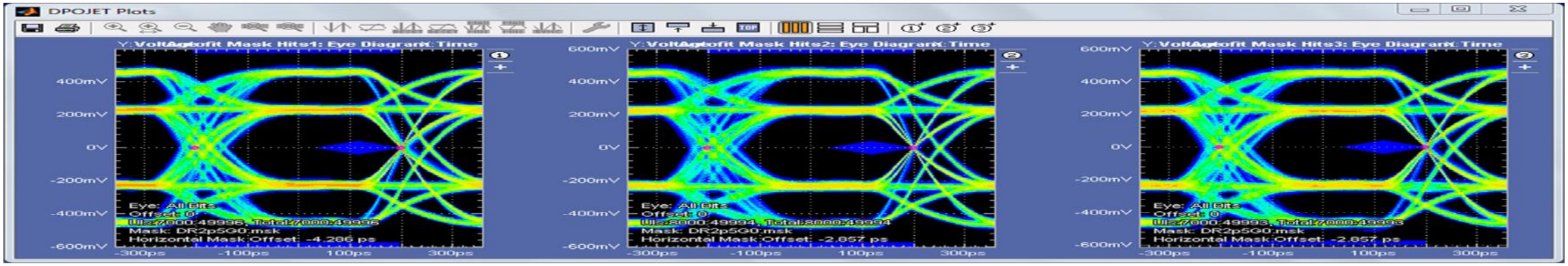
C-PHY Signaling



- (1) lane consists of (3) separate V_A, V_B, and V_C single-ended signals
- Bit encoding by TX, 16-bits → 7 symbols → three-wire state levels
- Differential RX sees three voltages as V_{AB}, V_{BC}, and V_{CA}
- Bits decoded by RX, three wire state levels → 7 symbols → 16-bits
- Co-exist on same pins used for D-PHY

C-PHY Transmitter Measurements

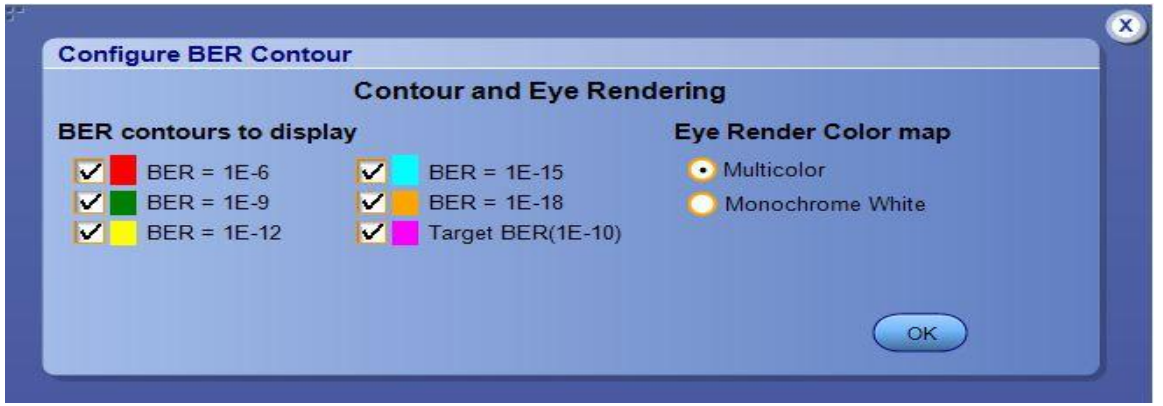
- 1st triggered edge recovered from A, B, and C wires
- Eye mask placement for optimal eye opening
- Jitter and eye diagram rendering performed over entire record length
- Rise/fall times specified for different transitions
- Embed or de-embed insertion loss and crosstalk from s-parameter file
- Acquire user specified # live waveforms, or process captured waveforms

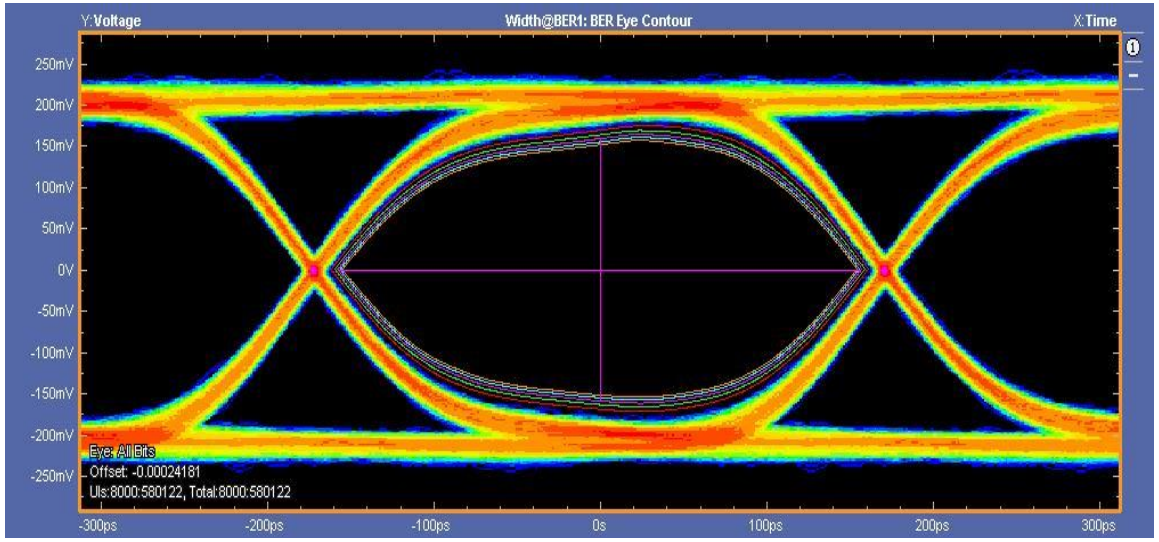


M-PHY Transmitter Measurements

- Total Jitter, Jitter Separation and Extrapolated Eye Analysis at 1E-10
- Slew Rate Testing
- Common Mode AC/DC tests
- Lane to Lane Skew
- Integration with Sig Test for Jitter Analysis and Correlation
- Power Spectral Density (Informative)
- PWM and SYS Mode tests

BER CONTOUR USING DPOJET

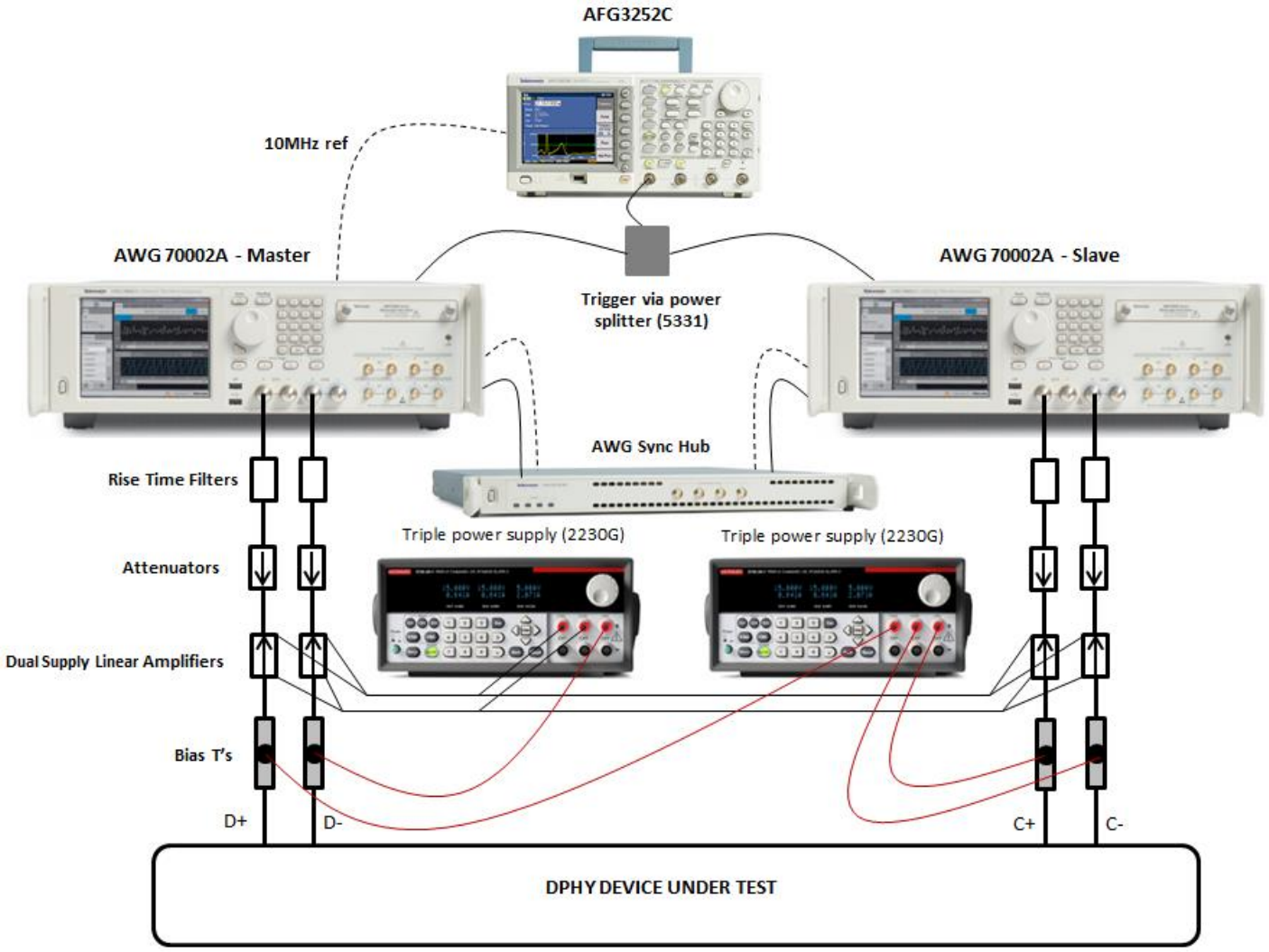




Receiver Test Overview

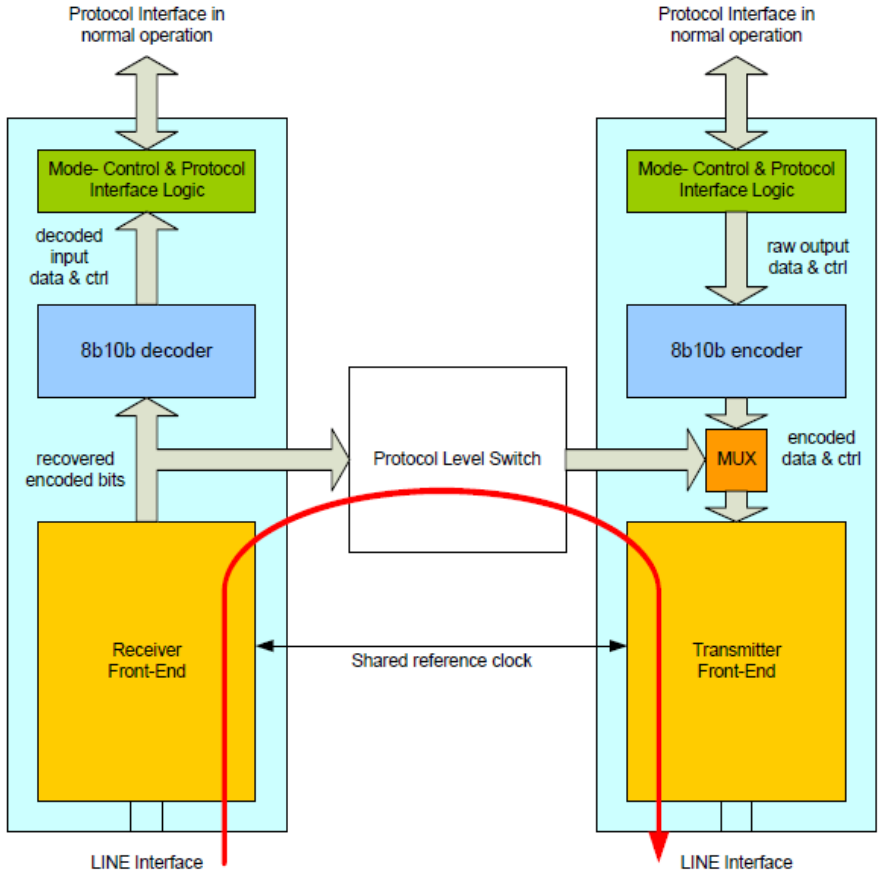
- D-PHY
  - Calibration for RX to be implemented in v2.0.
  - LP and HS modes
  - 35 tests including eSPIKE, CM/Diff voltage, Jitter Tolerance, Sj interference
- M-PHY
  - RX Calibration using Replica Trace, ISI Channel with Sj and Rj
  - PWM, SYS and HS modes
  - 32 tests including CM/Diff mode voltage, rise/fall time, UI, jitter, and eye diagram
- C-PHY
  - Data is three-wire single-ended, probe A & B & C on different scope channels
  - LP and HS modes
  - 24 tests including eSPIKE, CM/Diff voltage, Jitter Tolerance, Interference Tolerance

C-PHY & D-PHY RX Test Setup



M-PHY Receiver Measurements

- Stress calibration key to accurate RX testing
- Stressors include RT/FT, ISI, Rj, Sj, CM voltage, and differential eye height.
- JTOL and margin test at multiple Sj values
- Diff termination enable/disable tests
- Test at nominal bit rates +/- 2000ppm
- Stressed receiver testing
  - BERT
  - AWG + external error detector
- PWM & SYS Mode Testing with iBER



D-PHY Test Solutions

Electrical

D-PHY TX Essentials

Automated D-PHY TX

TX

D-PHY Express

Automated D-PHY RX

RX

HS Gear 2.5G D-PHY 1.2

D-PHY 2.0 4.5 G

Protocol Decode

DSI/CSI-2 Pattern Generator

DSI/CSI-2 Standalone Decoder

Scope-based Decoder

Specification Roadmap

C-PHY Test Solutions

Electrical

C-PHY TX Essentials

Automated C-PHY TX

C-PHY Express

Automated C-PHY RX

TX

RX

C-PHY 1.0

2.5GS/s

C-PHY 1.1

3.0 G

Protocol Decode

DSI/CSI-2 Pattern Generator

DSI/CSI-2 Standalone Decoder

Scope-based Decoder

Tektronix Internal Roadmap

Specification Roadmap

M-PHY Test Solutions

Electrical

- M-PHY TX Essentials
- Automated M-PHY TX
- Automated M-PHY RX

TX

RX

- M-PHY 3.0 — 5.8 Gbps
- M-PHY 4.0 — 11.6 Gbps

Protocol Decode

- DigiRF V4
- UFS, CSI-3, DSI UniPro
- SSIC
- MPCIe
- Sound Wire & I3C

Tektronix Internal Roadmap

Specification Roadmap

Tektronix Serial Standards Body Participation

John Calvin

Pavel Zivny

Rob Marsland

Oliver Kiehl

Anshuman Bhat

Tim Bieber

UN Vasudev

Tim Bieber

Kalev Sepp, PhD

Keyur Diwan

Yogesh Pai

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